

COMPAL CONFIDENTIAL

MODEL NAME : EDC42

PCB NO : LA-H171P

BOM P/N :

GPIO MAP: X10_WHL_KBL_CFLH_GPIO map Rev1.5_20180921

PWR Circuit: 14UMA_A00_PWR_20190308A

Brook Hollow 14 UMA (TBT)

Coffee Lake H

2019-03-20

REV : 1.0 (A00)

@ : Nopop Component

EMI@ : EMI Component

@EMI@ : EMI Nopop Component

ESD@ : ESD Component

@ESD@ : ESD Nopop Component

RF@ : RF Component

@RF@ : RF Nopop Component

XDP@ : XDP Component

CONN@ : Connector Component

5105@ : EC MEC5105 IC

5106@ : EC MEC5106 IC

WWAN@ : WWAN Component

WWANRF@ : WWAN RF Component

eSPI@ : eSPI interface

LPC@ : LPC interface

DS3@ : Deep sleep support

NDS3@ : non Deep sleep support

RTD3@ : RTD3 support

NRD3@ : non RTD3 support

VPRO@ : VPRO support

NVPRO@ : non VPRO support

ST33@ : ST33 TPM support

750@ : NPCT750 TPM support

JUMP@ : Jump solder and short

@JUMP@ : Jump no solder

SATAPERI@ : Pericom SATA repeater support

SATAPARA@ : Parade SATA repeater support

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Cover Sheet

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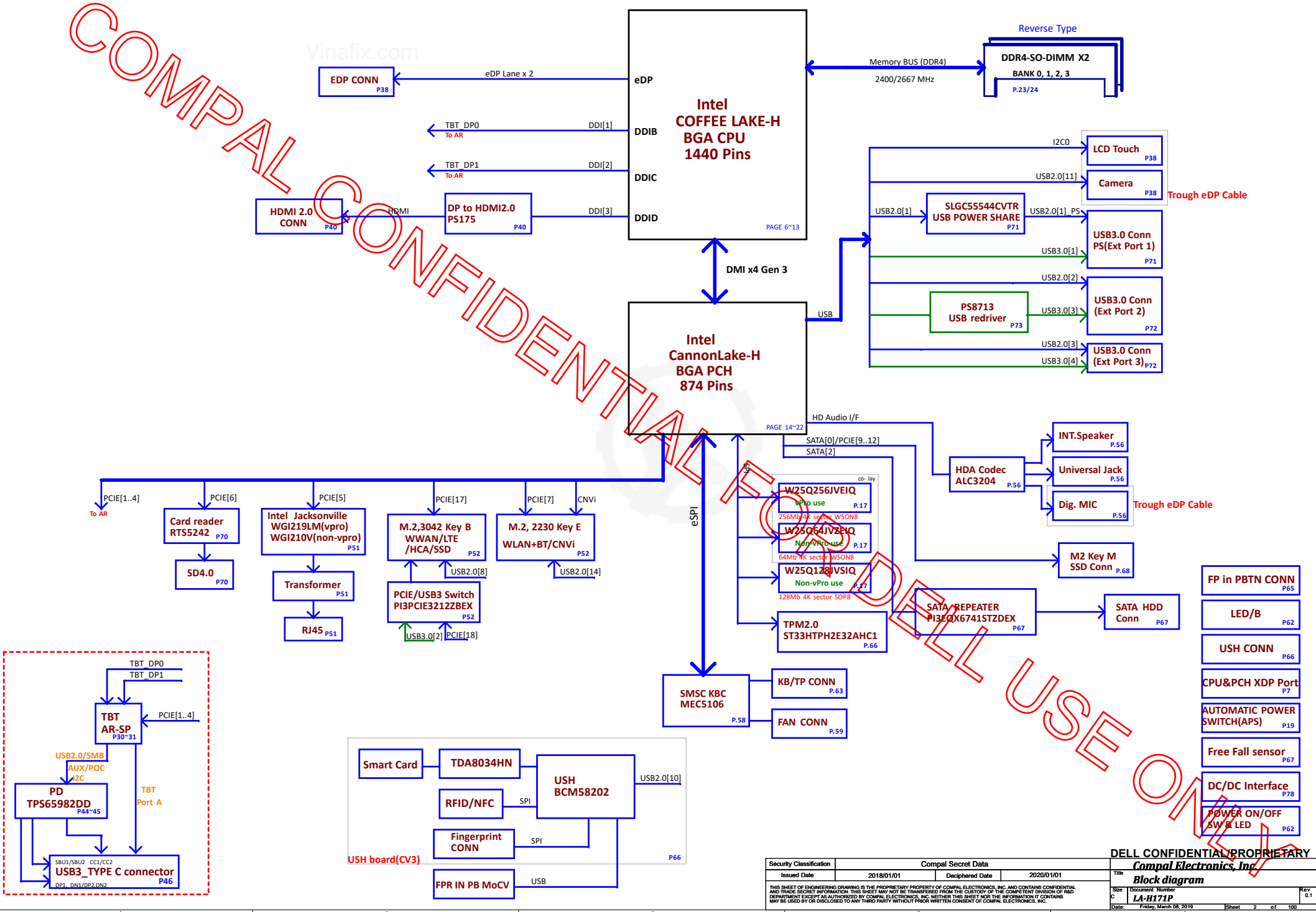
Part Number	Description
DAA000J2000	PCB 2FB LA-H171P REV0 MB 1

Layout Dell logo



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REV: A00
PWB: J11RG

Brook Hollow 14 UMA TBT Block Diagram



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_SUS +1.2V_MEM +1.0V_VCCST +2.5V_MEM	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.2V_RUN +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA +1.8V_RUN
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.50
			Add Plating		0.95
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080	2.60
2	GND1		Copper foil	1oz	1.35
		3.7	Core	4mil	4.00
3	Sig1		Copper foil	1oz	1.35
		3.6	Prepreg	2116HRCx2	2.90
4	GND1/PWR		Copper foil	1oz	1.35
		3.7	Core	4mil	4.00
5	Sig2		Copper foil	1oz	1.35
		3.6	Prepreg	2116HRCx2	2.20
6	Sig3		Copper foil	1oz	1.35
		3.6	Core	4mil	4.00
7	GND2		Copper foil	1oz	1.35
		3.7	Prepreg	1080	2.60
8	Bottom		Copper foil	0.5oz	0.65
			Add Plating		0.95
			SolderMask		0.50
Overall Thickness (1.2mm ± 10%)				47.2	46.60000
					1.18364

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	USB3.1 #8	USB3.1 #9	USB3.1 #10	PCIe #4	PCIe #5	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	SATA 1a	SATA 1b	PCIe #13	SATA 2	PCIe #14	SATA 3	PCIe #15	SATA 4	PCIe #16	SATA 5	PCIe #17	PCIe #18	PCIe #19
Intel® RST Support								No Support	No Support					Yes	No Support	Yes	Yes													

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USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC-1			JNGFF2-->M2 3042(LTE)
USB3.0-3	SSIC-2			JUSB2-->LEFT
USB3.0-4				JUSB3-->RIGHT
USB3.0-5				NA
USB3.0-6				NA
USB3.0-7		PCIE-1		Alpine Ridge - SP
USB3.0-8		PCIE-2		
USB3.0-9		PCIE-3		
USB3.0-10		PCIE-4		
		PCIE-5		LOM
		PCIE-6		Card Reader
		PCIE-7		JNGFF1-->M.2 2230(WLAN)
		PCIE-8		NA
		PCIE-9		M.2 Socket 3 (Key M) M.2 2280 SSD (PCIex4 or SATA)
		PCIE-10	SATA-0A	
		PCIE-11	SATA-1A	
		PCIE-12	SATA-1A	
		PCIE-13	SATA-0B	NA
		PCIE-14	SATA-1B	NA
		PCIE-15	SATA-2	JSATA1-->HDD SATA
		PCIE-16	SATA-3	NA
		PCIE-17	SATA-4	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-18	SATA-5	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-19		NA
		PCIE-20		NA

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2 -->LEFT
3	JUSB3-->RIGHT
4	FP IN PB
5	TI PD
6	test point
7	NA
8	JNGFF2-->M2 3042(WWAN)
9	NA
10	JUSH1-->USH
11	JEDP1-->Camera
12	NA
13	NA
14	JNGFF1--> M.2 2230(CNVi_BT)

USH	H	BIO
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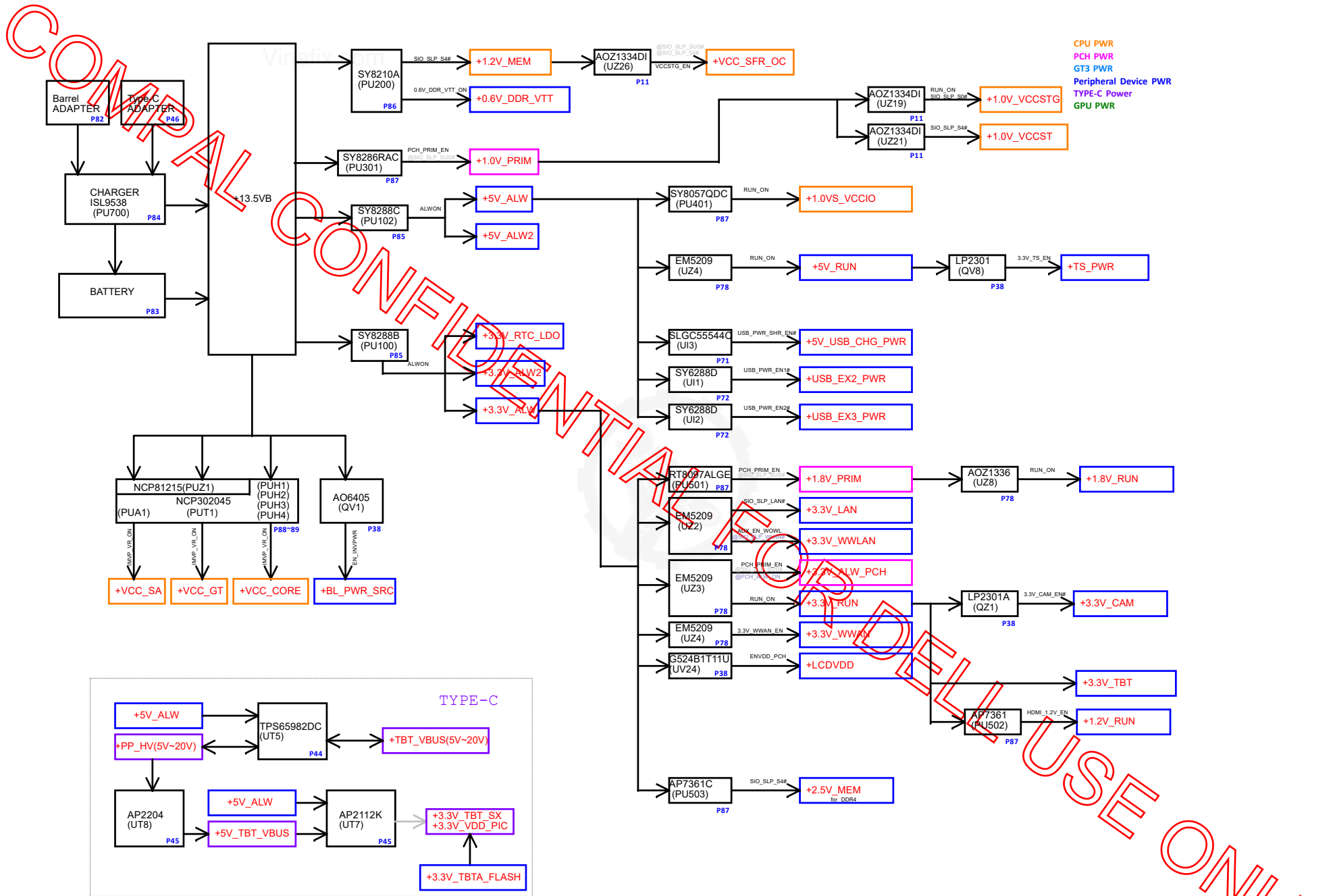
VIDEO	DESTINATION
eDP	LCD
DDI-B	Alpine Ridge - SP (Port 0)
DDI-C	Alpine Ridge - SP (Port 1)
DDI-D	PS175 --> JHDMI1

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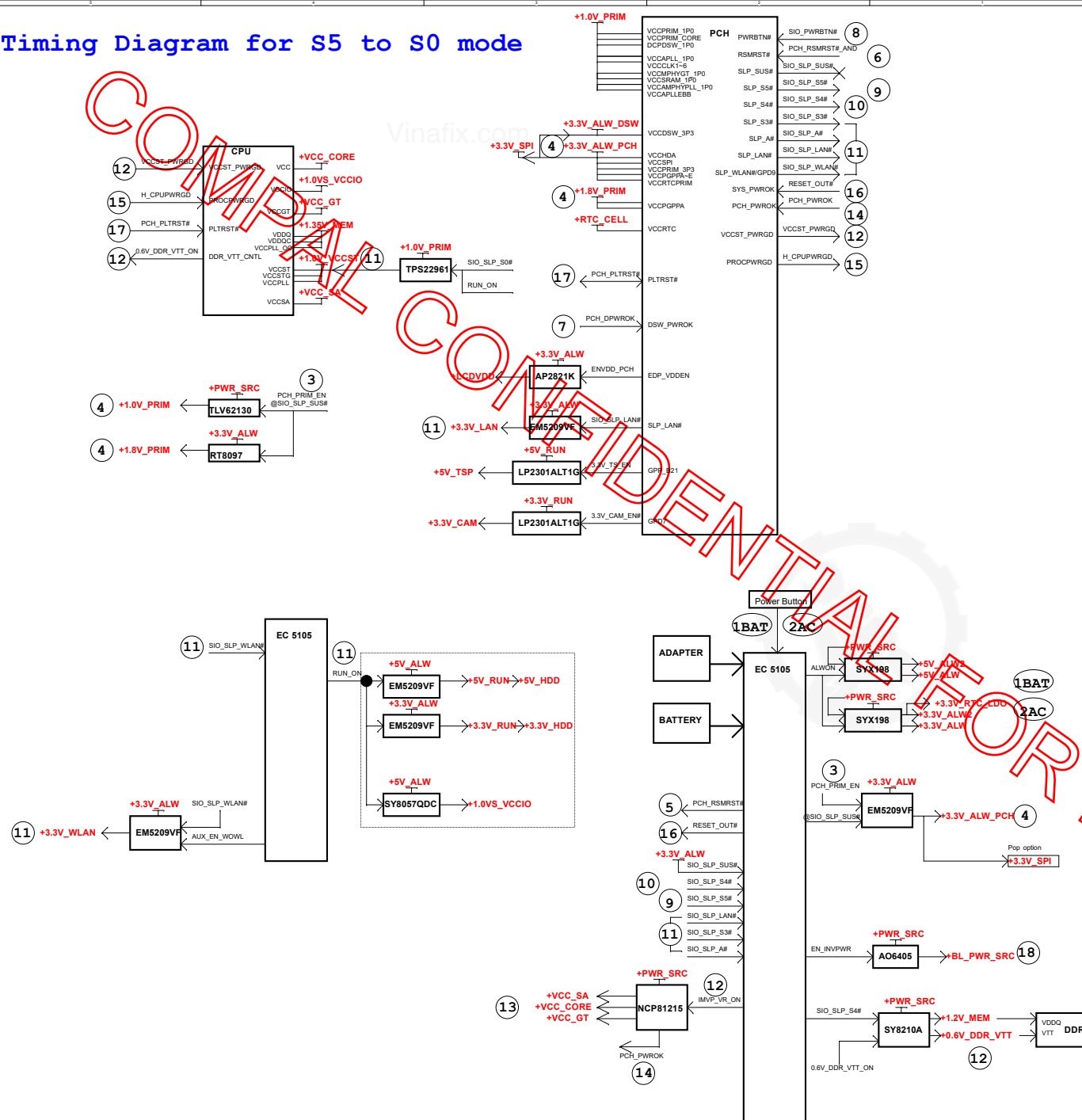
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Port Assignment

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Timing Diagram for S5 to S0 mode



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CFG11

DMI_AC_coupled	
HALF-SWING DC coupled	1
FULL-SWING AC coupling	0

CFG10

SAFE mode boot	
active	1
Not active	0

CFG12

PMSYNC2.0	
	1
LEGACY	0

CFG9

SVID NOT Present	
Present	1
Not presnet	0

CFG8

CFG UNLOCK	
disable	1
enable	0

CFG1

PCHLESS MODE (CRB) Reserved CFG lane (EDS)	
NORMAL	1
PCHLESS	0

CFG13

SYNC & AYNC MODE	
ASYNCHRONOUS	1
SYNCHRONOUS	0

CFG0

Stall reset sequence after PCU PLL lock until de-asserted	
No Stall	1
Stall	0

CFG2

PEG LANE REVERSAL	
NORMAL	1
LANE REVERSED	0

CFG4

eDP enable	
Disabled	1
Enabled	0

CFG5

PCI Express* Bifurcation [6:5]	
1x8, 2x4	00
Reserved	01
2x8	10
1x16	11

CFG6

PEG Training	
PEG Training immediately following BIOS de-assertion	1
PEG Training for BIOS for training	0

CFG19

SAFE mode boot	
active	1
Not active	0

CFG18

SAFE mode boot	
active	1
Not active	0

CFG17

SAFE mode boot	
active	1
Not active	0

CFG16

SAFE mode boot	
active	1
Not active	0

CFG15

SAFE mode boot	
active	1
Not active	0

CFG14

SAFE mode boot	
active	1
Not active	0

CFG13

SAFE mode boot	
active	1
Not active	0

CFG12

SAFE mode boot	
active	1
Not active	0

CFG11

SAFE mode boot	
active	1
Not active	0

CFG10

SAFE mode boot	
active	1
Not active	0

CFG9

SAFE mode boot	
active	1
Not active	0

CFG8

SAFE mode boot	
active	1
Not active	0

CFG7

SAFE mode boot	
active	1
Not active	0

CFG6

SAFE mode boot	
active	1
Not active	0

CFG5

SAFE mode boot	
active	1
Not active	0

CFG4

SAFE mode boot	
active	1
Not active	0

CFG3

SAFE mode boot	
active	1
Not active	0

CFG2

SAFE mode boot	
active	1
Not active	0

CFG1

SAFE mode boot	
active	1
Not active	0

CFG0

SAFE mode boot	
active	1
Not active	0

CFG19

SAFE mode boot	
active	1
Not active	0

CFG18

SAFE mode boot	
active	1
Not active	0

CFG17

SAFE mode boot	
active	1
Not active	0

CFG16

SAFE mode boot	
active	1
Not active	0

CFG15

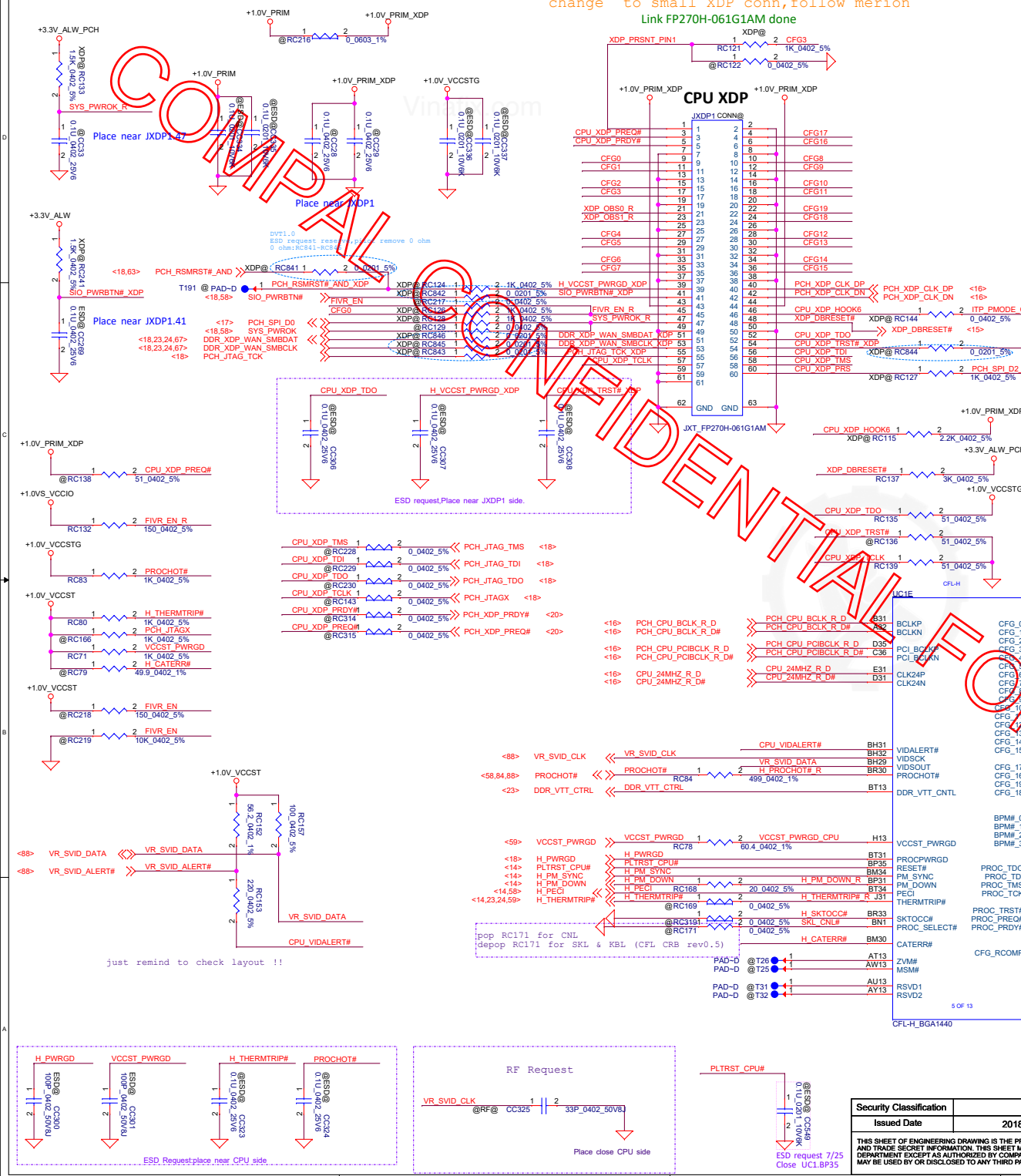
SAFE mode boot	
active	1
Not active	0

CFG14

SAFE mode boot	
active	1
Not active	0

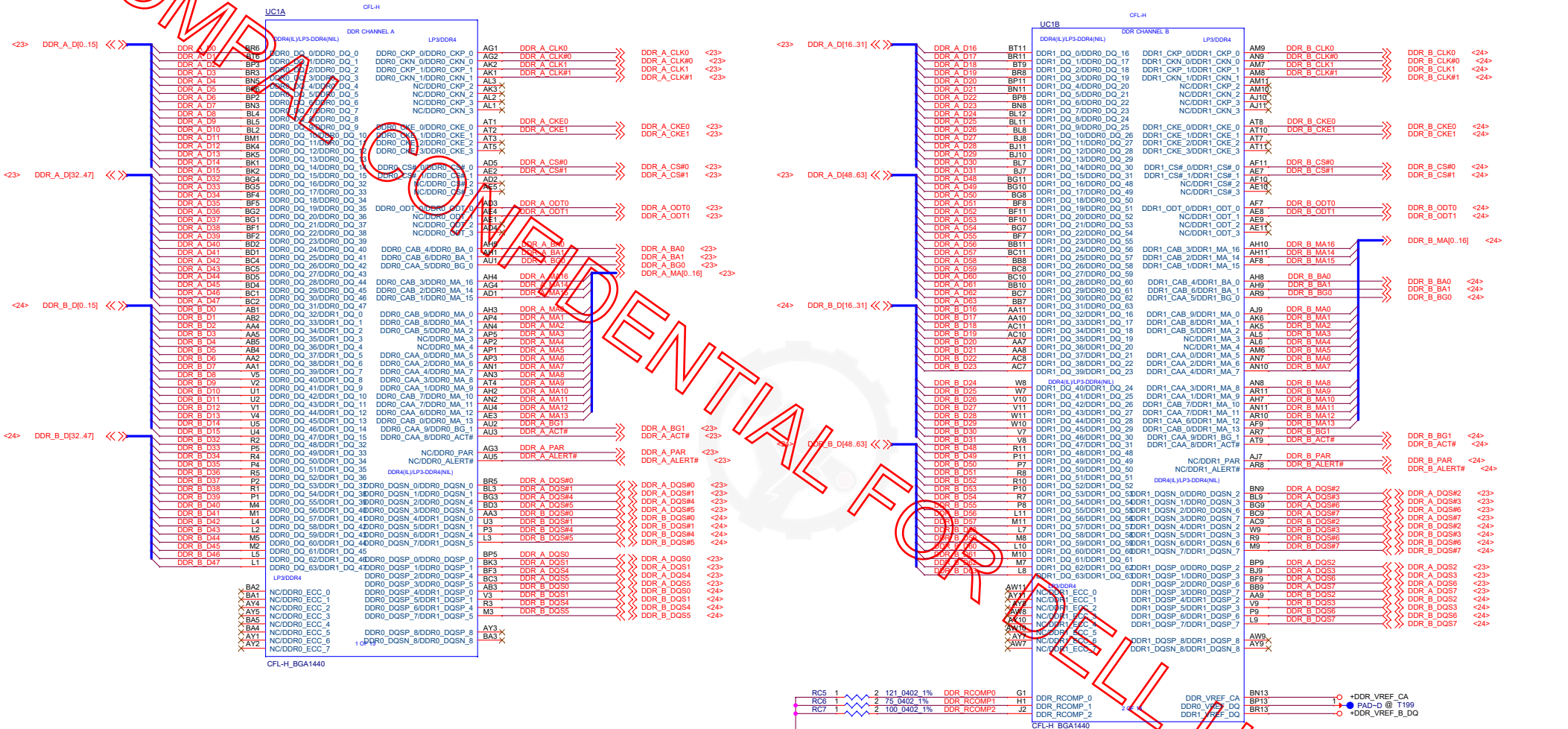
CFG13

||
||
||



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Trace width=12-15 mils
Spacing=20mil
Max length= 500 mils.

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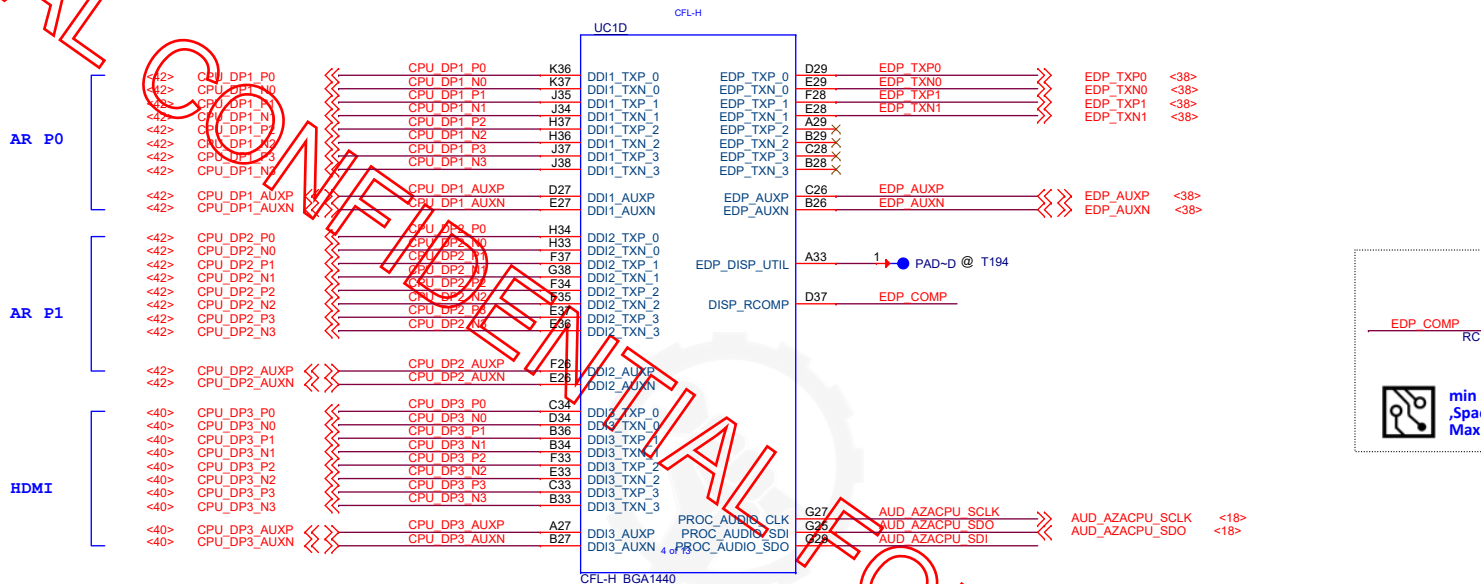
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CFL-H (3/8)

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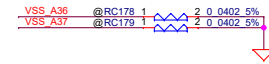
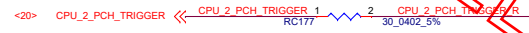


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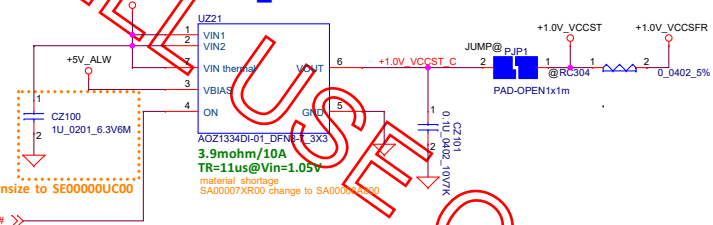
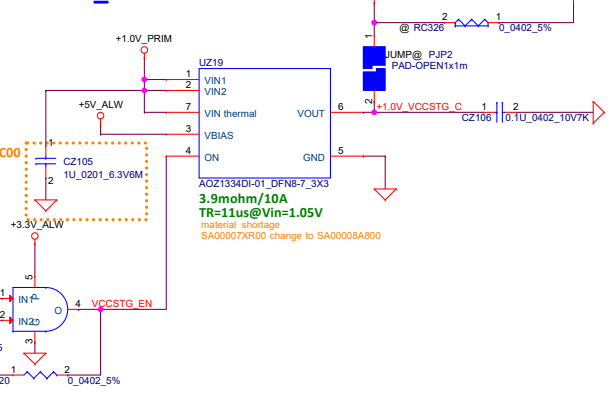
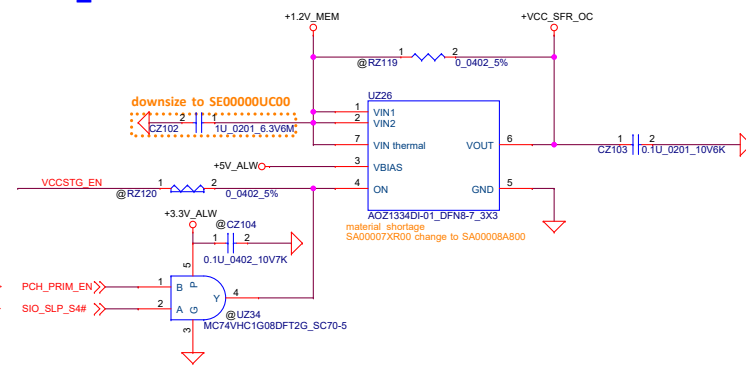
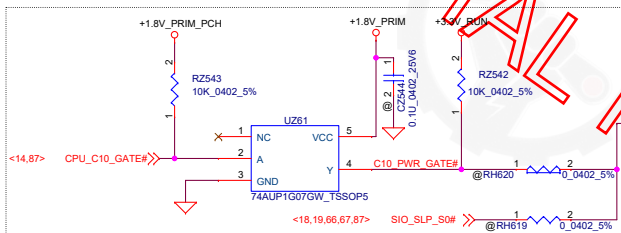
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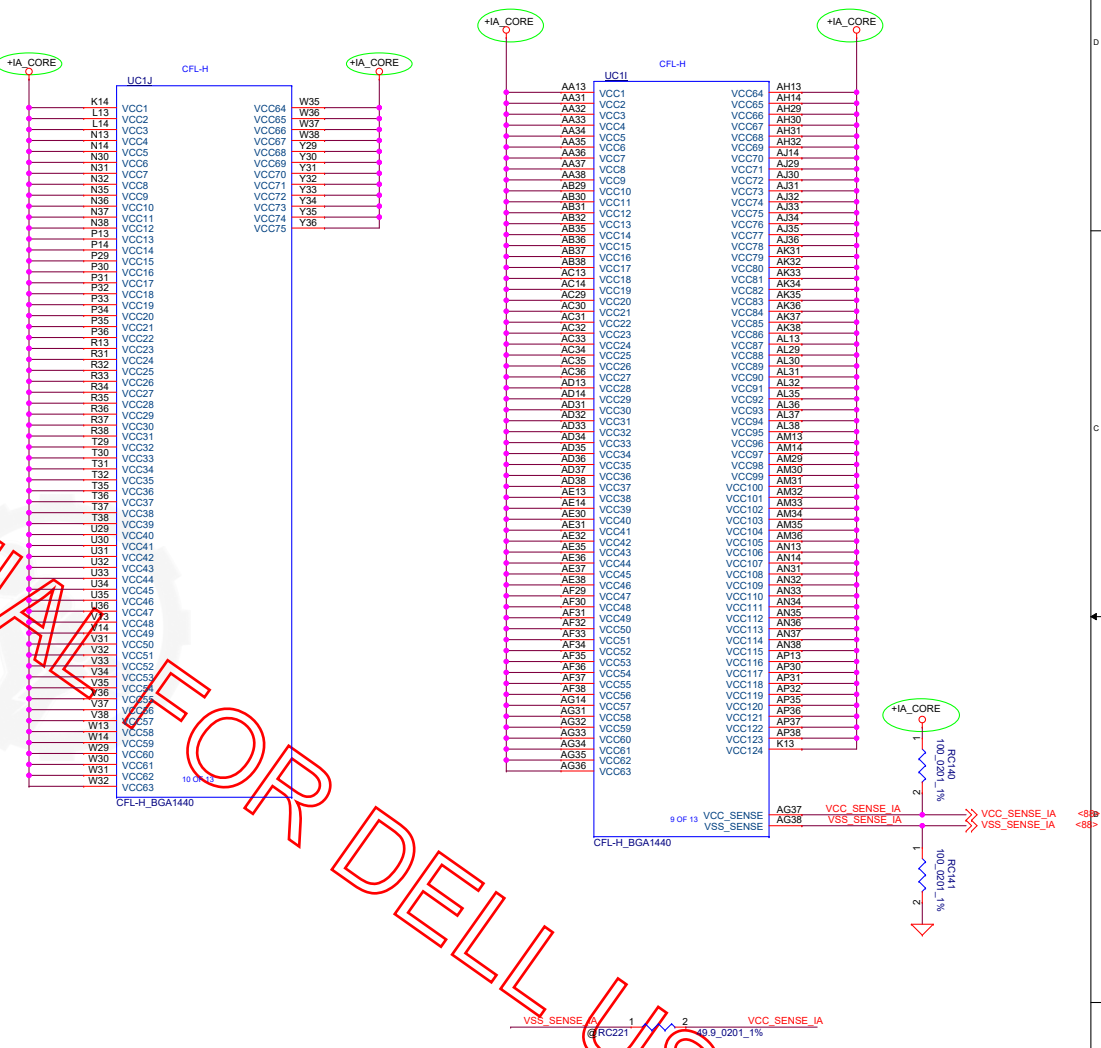
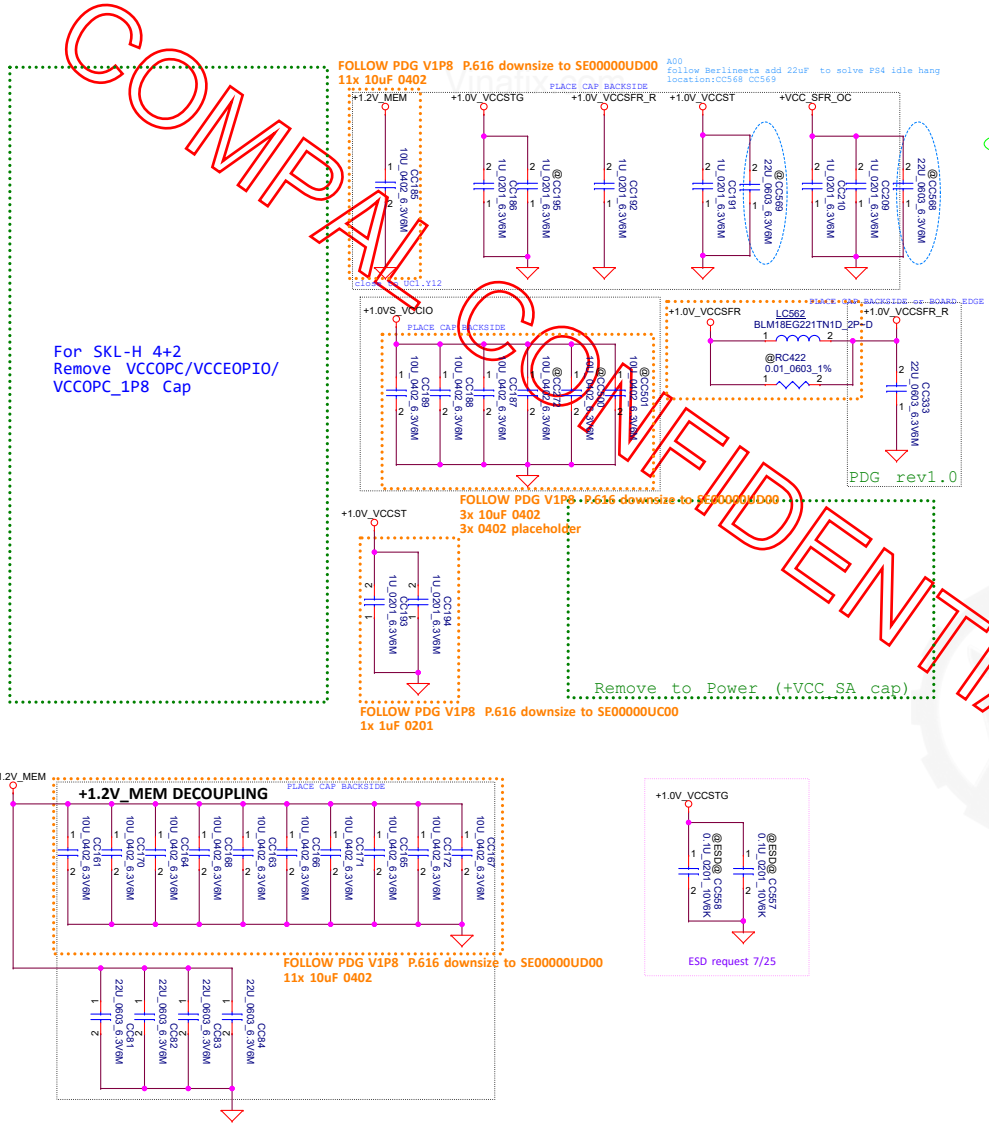
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CFL-H		
UC1F		AK4
A10	VSS 1	VSS 82
A12	VSS 2	VSS 83
A16	VSS 3	VSS 84
A18	VSS 4	VSS 85
A20	VSS 5	VSS 86
A22	VSS 6	VSS 87
A24	VSS 7	VSS 88
A26	VSS 8	VSS 89
A28	VSS 9	VSS 90
A30	VSS 10	VSS 91
A32	VSS 11	VSS 92
A34	VSS 12	VSS 93
AA29	VSS 13	VSS 94
AA30	VSS 14	VSS 95
AB33	VSS 15	VSS 96
AB34	VSS 16	VSS 97
AB6	VSS 17	VSS 98
AC1	VSS 18	VSS 99
AC12	VSS 19	VSS 100
AC2	VSS 20	VSS 101
AC3	VSS 21	VSS 102
AC37	VSS 22	VSS 103
AC38	VSS 23	VSS 104
AC4	VSS 24	VSS 105
AC5	VSS 25	VSS 106
AC6	VSS 26	VSS 107
AD10	VSS 27	VSS 108
AD11	VSS 28	VSS 109
AD12	VSS 29	VSS 110
AD29	VSS 30	VSS 111
AD30	VSS 31	VSS 112
AD6	VSS 32	VSS 113
AD8	VSS 33	VSS 114
AD9	VSS 34	VSS 115
AE33	VSS 35	VSS 116
AE34	VSS 36	VSS 117
AE6	VSS 37	VSS 118
AF1	VSS 38	VSS 119
AF12	VSS 39	VSS 120
AF13	VSS 40	VSS 121
AF14	VSS 41	VSS 122
AF2	VSS 42	VSS 123
AF3	VSS 43	VSS 124
AF4	VSS 44	VSS 125
AG10	VSS 45	VSS 126
AG11	VSS 46	VSS 127
AG13	VSS 47	VSS 128
AG29	VSS 48	VSS 129
AG30	VSS 49	VSS 130
AG6	VSS 50	VSS 131
AG7	VSS 51	VSS 132
AG8	VSS 52	VSS 133
AH12	VSS 53	VSS 134
AH33	VSS 54	VSS 135
AH34	VSS 55	VSS 136
AH36	VSS 56	VSS 137
AH6	VSS 57	VSS 138
AJ1	VSS 58	VSS 139
AJ13	VSS 59	VSS 140
AJ2	VSS 60	VSS 141
AJ3	VSS 61	VSS 142
AJ37	VSS 62	VSS 143
AJ38	VSS 63	VSS 144
AJ4	VSS 64	VSS 145
AJ5	VSS 65	VSS 146
AJ6	VSS 66	VSS 147
W4	VSS 67	VSS 148
W5	VSS 68	VSS 149
Y10	VSS 69	VSS 150
Y11	VSS 70	VSS 151
Y13	VSS 71	VSS 152
Y14	VSS 72	VSS 153
Y37	VSS 73	VSS 154
Y38	VSS 74	VSS 155
Y7	VSS 75	VSS 156
Y8	VSS 76	VSS 157
Y9	VSS 77	VSS 158
W3	VSS 78	VSS 159
W33	VSS 79	VSS 160
W34	VSS 80	VSS 161
W34	VSS 81	VSS 162

CFL-H_BGA1440

CFL-H		
UC1G		BJ15
AW5	VSS 163	VSS 244
AY12	VSS 164	VSS 245
AY33	VSS 165	VSS 246
AY34	VSS 166	VSS 247
B9	VSS 167	VSS 248
BA10	VSS 168	VSS 249
BA12	VSS 169	VSS 250
BA37	VSS 170	VSS 251
BA38	VSS 171	VSS 252
BA6	VSS 172	VSS 253
BA7	VSS 173	VSS 254
BA8	VSS 174	VSS 255
BA9	VSS 175	VSS 256
BB1	VSS 176	VSS 257
BB12	VSS 177	VSS 258
BB2	VSS 178	VSS 259
BB3	VSS 179	VSS 260
BB29	VSS 180	VSS 261
BB3	VSS 181	VSS 262
BB4	VSS 182	VSS 263
BB5	VSS 183	VSS 264
BB6	VSS 184	VSS 265
BC12	VSS 185	VSS 266
BC13	VSS 186	VSS 267
BC14	VSS 187	VSS 268
BC33	VSS 188	VSS 269
BC34	VSS 189	VSS 270
BC6	VSS 190	VSS 271
BD10	VSS 191	VSS 272
BD11	VSS 192	VSS 273
BD12	VSS 193	VSS 274
BD7	VSS 194	VSS 275
BD8	VSS 195	VSS 276
BD9	VSS 196	VSS 277
BD8	VSS 197	VSS 278
BD9	VSS 198	VSS 279
BE	VSS 199	VSS 280
BE	VSS 200	VSS 281
BE29	VSS 201	VSS 282
BE3	VSS 202	VSS 283
BE3	VSS 203	VSS 284
BE4	VSS 204	VSS 285
BE5	VSS 205	VSS 286
BE5	VSS 206	VSS 287
BF12	VSS 207	VSS 288
BF33	VSS 208	VSS 289
BF34	VSS 209	VSS 290
BF6	VSS 210	VSS 291
BG12	VSS 211	VSS 292
BG13	VSS 212	VSS 293
BG14	VSS 213	VSS 294
BG37	VSS 214	VSS 295
BG38	VSS 215	VSS 296
BG6	VSS 216	VSS 297
BH1	VSS 217	VSS 298
BH10	VSS 218	VSS 299
BH11	VSS 219	VSS 300
BH12	VSS 220	VSS 301
BH14	VSS 221	VSS 302
BH2	VSS 222	VSS 303
BH3	VSS 223	VSS 304
BH4	VSS 224	VSS 305
BH5	VSS 225	VSS 306
BH6	VSS 226	VSS 307
BH7	VSS 227	VSS 308
BH8	VSS 228	VSS 309
BH9	VSS 229	VSS 310
T2	VSS 230	VSS 311
T3	VSS 231	VSS 312
T3	VSS 232	VSS 313
T34	VSS 233	VSS 314
T4	VSS 234	VSS 315
T5	VSS 235	VSS 316
T7	VSS 236	VSS 317
T8	VSS 237	VSS 318
T9	VSS 238	VSS 319
U37	VSS 239	VSS 320
U38	VSS 240	VSS 321
U38	VSS 241	VSS 322
U38	VSS 242	VSS 323
U38	VSS 243	VSS 324

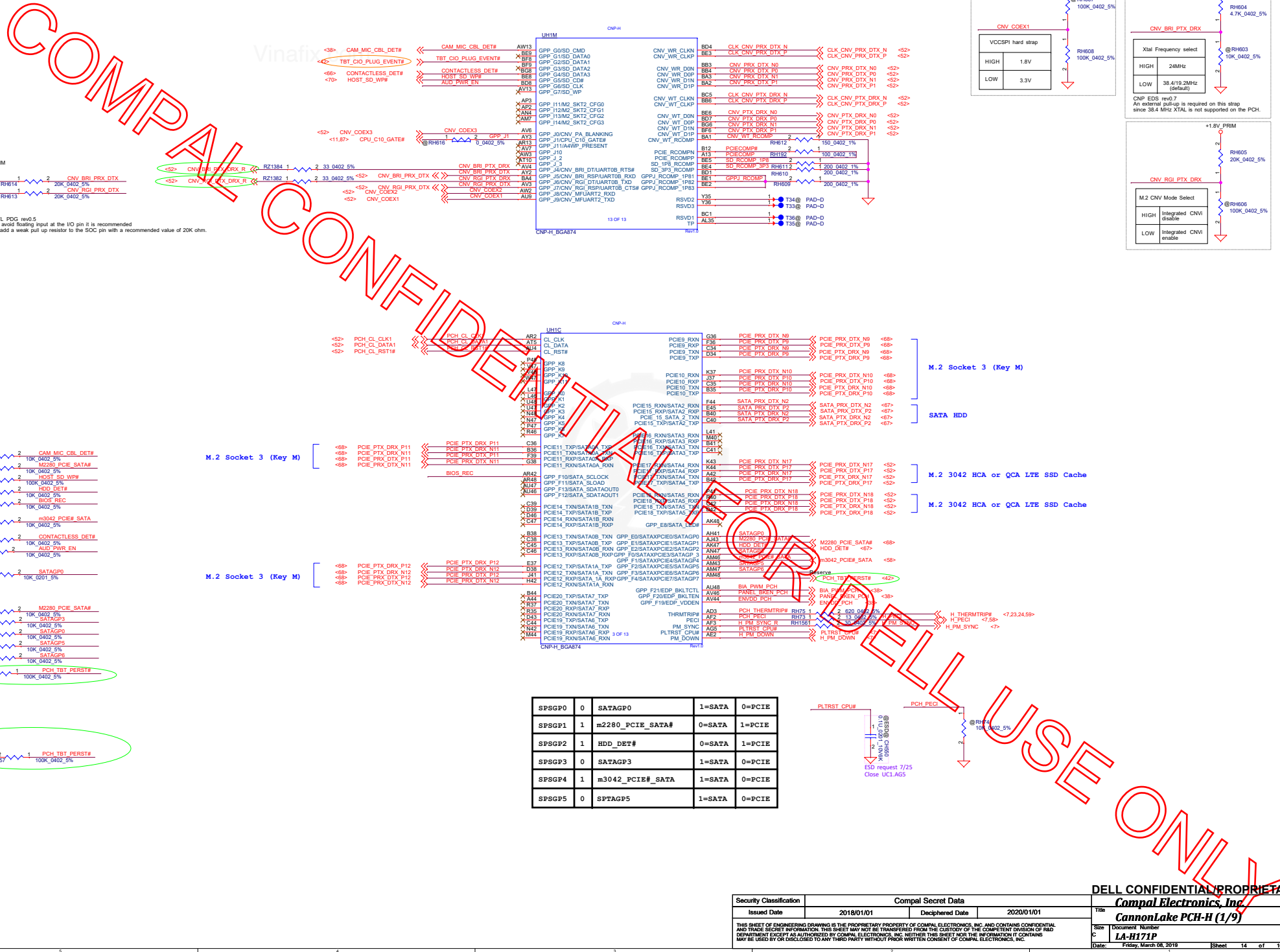
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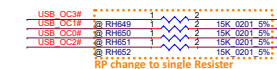
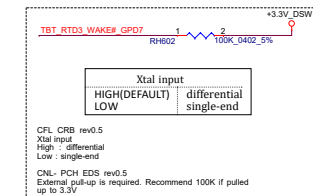
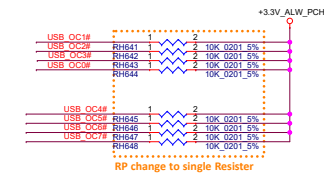
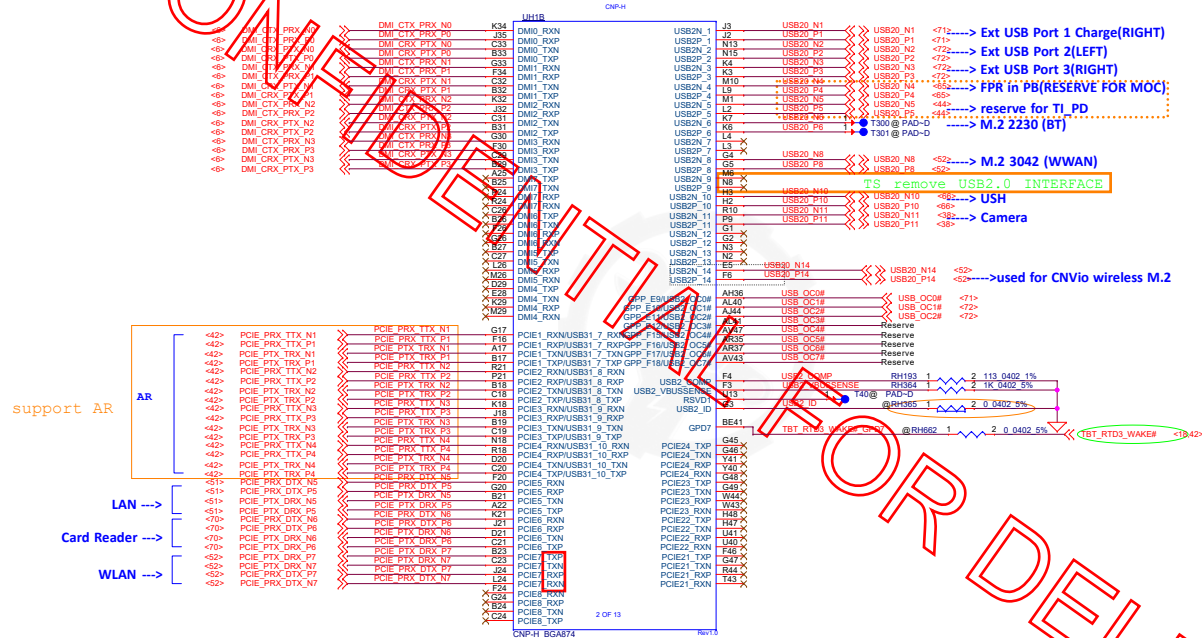
CFL-H		
UC1H		F15
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BN7	VSS 326	VSS 410
BP12	VSS 327	VSS 411
BP14	VSS 328	VSS 412
BP18	VSS 329	VSS 413
BP21	VSS 330	VSS 414
BP26	VSS 331	VSS 415
BP26	VSS 332	VSS 416
BP26	VSS 333	VSS 417
BP29	VSS 334	VSS 418
BP33	VSS 335	VSS 419
BP34	VSS 336	VSS 420
BP7	VSS 337	VSS 421
BR12	VSS 338	VSS 422
BR14	VSS 339	VSS 423
BR18	VSS 340	VSS 424
BR21	VSS 341	VSS 425
BR24	VSS 342	VSS 426
BR25	VSS 343	VSS 427
BR26	VSS 344	VSS 428
BR29	VSS 345	VSS 429
BR34	VSS 346	VSS 430
BR36	VSS 347	VSS 431
BR7	VSS 348	VSS 432
BT12	VSS 349	VSS 433
BT14	VSS 350	VSS 434
BT18	VSS 351	VSS 435
BT21	VSS 352	VSS 436
BT24	VSS 353	VSS 437
BT26	VSS 354	VSS 438
BT29	VSS 355	VSS 439
BT32	VSS 356	VSS 440
BT5	VSS 357	VSS 441
C11	VSS 358	VSS 442
C13	VSS 359	VSS 443
C15	VSS 360	VSS 444
C17	VSS 361	VSS 445
C19	VSS 362	VSS 446
C21	VSS 363	VSS 447
C23	VSS 364	VSS 448
C25	VSS 365	VSS 449
C27	VSS 366	VSS 450
C29	VSS 367	VSS 451
C31	VSS 368	VSS 452
C37	VSS 369	VSS 453
C5	VSS 370	VSS 454
C8	VSS 371	VSS 455
C9	VSS 372	VSS 456
D10	VSS 373	VSS 457
D12	VSS 374	VSS 458
D16	VSS 375	VSS 459
D18	VSS 376	VSS 460
D20	VSS 377	VSS 461
D24	VSS 378	VSS 462
D25	VSS 379	VSS 463
D26	VSS 380	VSS 464
D28	VSS 381	VSS 465
D3	VSS 382	VSS 466
D30	VSS 383	VSS 467
D33	VSS 384	VSS 468
D6	VSS 385	VSS 469
D9	VSS 386	VSS 470
E34	VSS 387	VSS 471
E35	VSS 388	VSS 472
E38	VSS 389	VSS 473
E4	VSS 390	VSS 474
E9	VSS 391	VSS 475
N3	VSS 392	VSS 476
N33	VSS 393	VSS 477
N34	VSS 394	VSS 478
N4	VSS 395	VSS 479
N5	VSS 396	VSS 480
N6	VSS 397	VSS 481
N7	VSS 398	VSS 482
N9	VSS 399	VSS 483
N9	VSS 400	VSS 484
P12	VSS 401	VSS 485
P37	VSS 402	VSS 486
M12	VSS 403	VSS 487
M6	VSS 404	VSS 488
N1	VSS 405	VSS 489
F11	VSS 406	VSS 490
F13	VSS 407	VSS 491
F13	VSS 408	VSS 492

CFL-H_BGA1440

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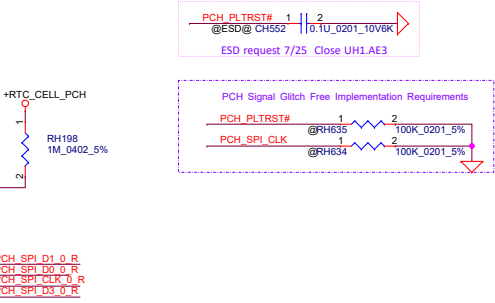
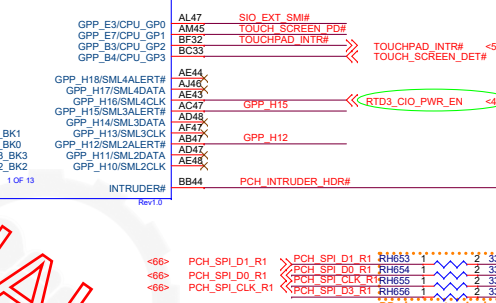
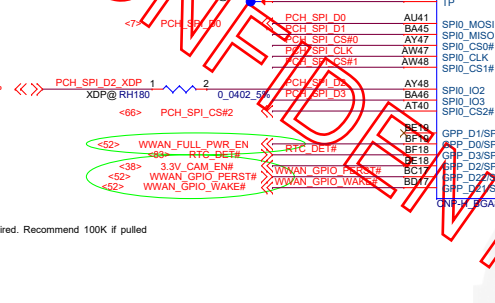
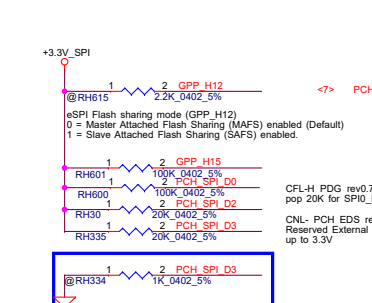
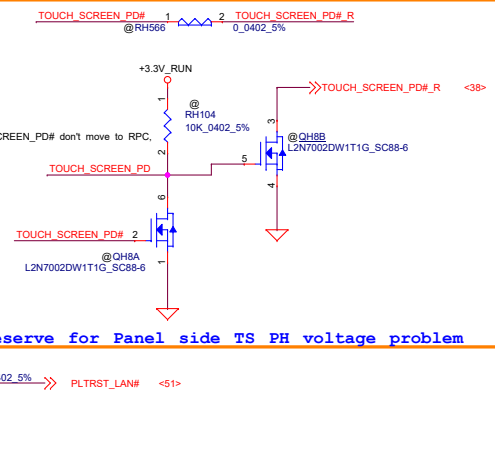
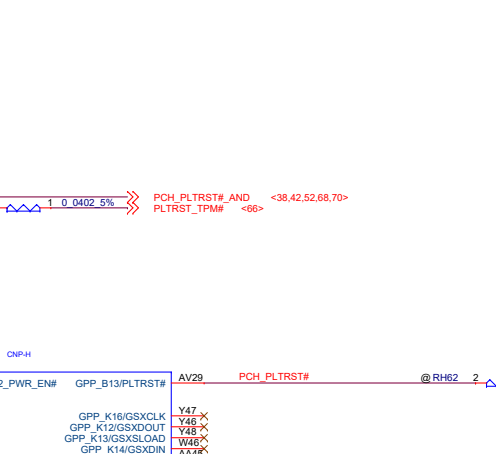
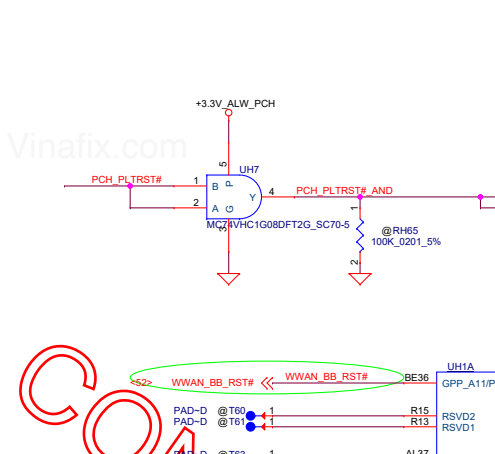
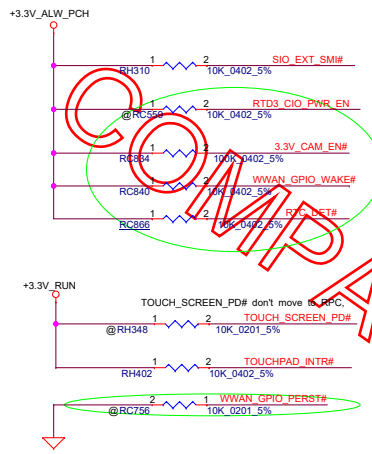
Security Classification		Compal Secret Data		DELETED CONFIDENTIAL/NOT FOR RELEASE Compal Electronics, Inc.		
Issued Date	2018/01/01	Deciphered Date	2020/01/01	Title	CFL-H (8/8)	
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				A	LA-H171P	
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CannonLake PCH-H (2/9)

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Issued Date	2018/01/01	Deciphered Date	2020/01/01	
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Size	Document Number		Rev	
	LA-H171P			
Date:	Monday, March 11, 2019	Sheet	15	of 100



9/5 MOW
Opt on 11 mpe nert a 1k Ohm pul-down resistor on the signal and de populatethe
required 1k Ohm pull-up resistor. In this case, customers must ensure that the SPI
flash device on the platform has HOLD function it disabled by default

Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platform
with ES and SKL S/H platform with pre ES/ES1sa mpe ns

For vPro
32MB WSON8 Flash ROM
For Non-vPro
8MB WSON8 Flash ROM

ESPI

	VPRO	NVRRO
RH178, RH179, RH181, RH183, RH184	5 ohm	10 ohm

For Non-vPro
16MB SOP8 Flash ROM

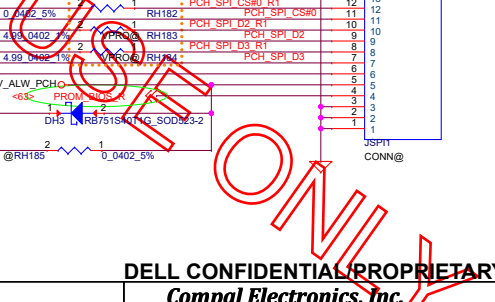
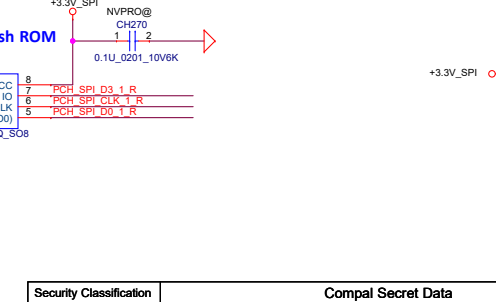
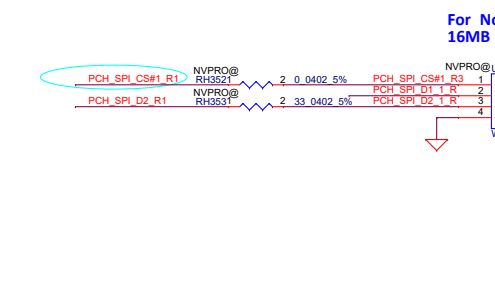
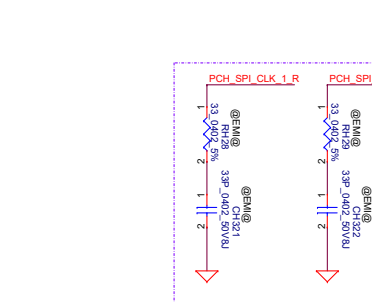
ESPI

	VPRO	NVRRO
RH178, RH179, RH181, RH183, RH184	5 ohm	10 ohm

VPRO PDG P.357 R2 5 ohm
NVRPRO PDG P.359 R2 10 ohm
RH178, RH179, RH181, RH183, RH184
NVRPRO BOM OPTION IN PAGE 61

JSPI1 follow KKW, for H limit

	VPRO	NVRRO
RH178, RH179, RH181, RH183, RH184	5 ohm	10 ohm



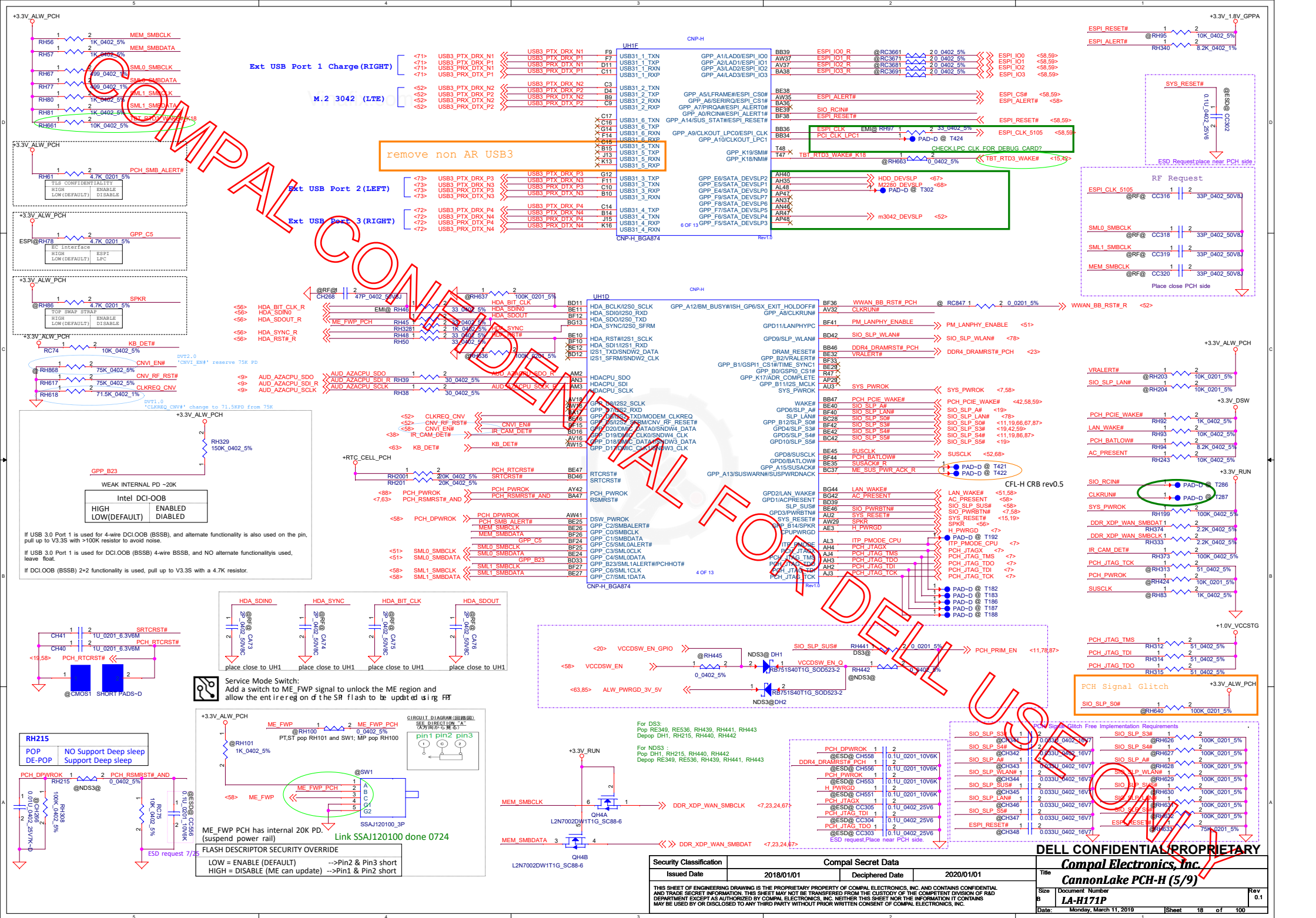
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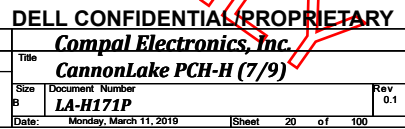
Compal Electronics, Inc.

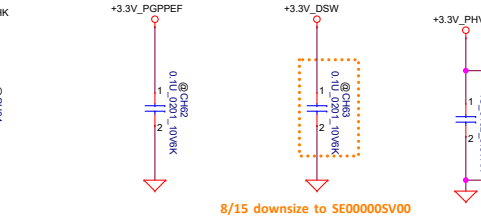
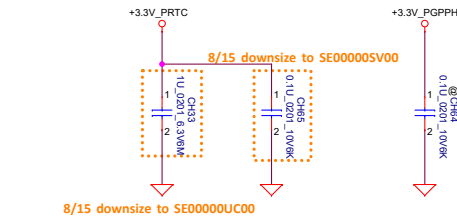
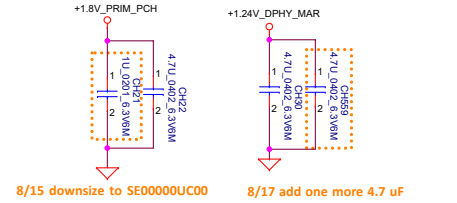
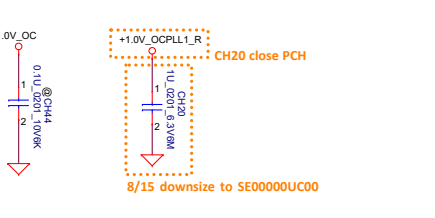
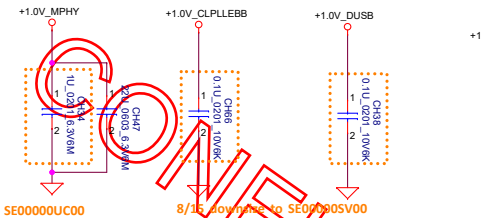
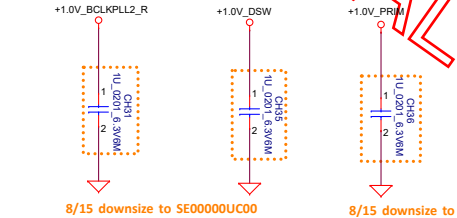
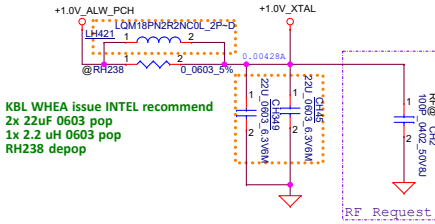
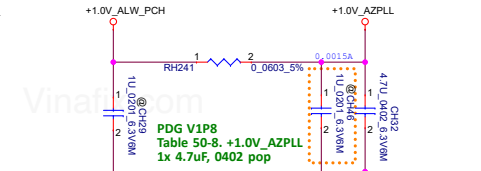
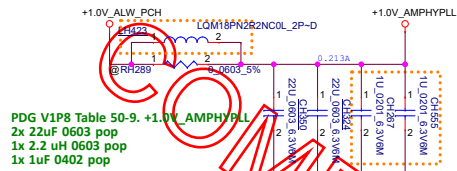
CannonLake PCH-H (4/9)

Security Classification	Compal Secret Data
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Deciphered Date	2020/01/01

Size	Document Number	Rev
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CFL-H PDG rev0.5
4.7uF x1
CRB-H rev0.7
0.1uF x1, 1uF x1

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CannonLake PCH-H (8/9)			
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B	LA-H171P	0.1	
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CNP-H

UH1L

A2	VSS_1	VSS_73	AL17
A28	VSS_2	VSS_74	AL21
A3	VSS_3	VSS_75	AL24
A33	VSS_4	VSS_76	AL26
A37	VSS_5	VSS_77	AL28
A4	VSS_6	VSS_78	AL33
A46	VSS_7	VSS_79	AL38
A47	VSS_8	VSS_80	AM1
A48	VSS_9	VSS_81	AM18
A5	VSS_10	VSS_82	AM32
A55	VSS_11	VSS_83	AM40
A56	VSS_12	VSS_84	AN12
AA19	VSS_13	VSS_85	AN16
AA20	VSS_14	VSS_86	AN18
AA25	VSS_15	VSS_87	AP28
AA27	VSS_16	VSS_88	AP4
AA28	VSS_17	VSS_89	AP9
AA30	VSS_18	VSS_90	AR32
AA31	VSS_19	VSS_91	AR10
AA49	VSS_20	VSS_92	AS4
AA5	VSS_21	VSS_93	AS8
AB19	VSS_22	VSS_94	AT1
AB25	VSS_23	VSS_95	AT16
AB31	VSS_24	VSS_96	AT18
AC12	VSS_25	VSS_97	AT21
AC17	VSS_26	VSS_98	AT24
AC33	VSS_27	VSS_99	AT26
AC38	VSS_28	VSS_100	AT28
AD1	VSS_29	VSS_101	AV39
AD2	VSS_30	VSS_102	AW10
AD19	VSS_31	VSS_103	AW4
AD2	VSS_32	VSS_104	AW40
AD22	VSS_33	VSS_105	B47
AD25	VSS_34	VSS_106	B48
AD49	VSS_35	VSS_107	B49
AE12	VSS_36	VSS_108	BA12
AE33	VSS_37	VSS_109	BA14
AE38	VSS_38	VSS_110	BA44
AE4	VSS_39	VSS_111	BA5
AE46	VSS_40	VSS_112	BA6
AF22	VSS_41	VSS_113	BB41
AF25	VSS_42	VSS_114	BB9
AF28	VSS_43	VSS_115	BC10
AG1	VSS_44	VSS_116	BC15
AG22	VSS_45	VSS_117	BC18
AG23	VSS_46	VSS_118	BC24
AG25	VSS_47	VSS_119	BC26
AG27	VSS_48	VSS_120	BC31
AG28	VSS_49	VSS_121	BC35
AG30	VSS_50	VSS_122	BC40
AG49	VSS_51	VSS_123	BC45
AH12	VSS_52	VSS_124	BD3
AH17	VSS_53	VSS_125	BD44
AH33	VSS_54	VSS_126	BE1
AH38	VSS_55	VSS_127	BE2
AJ19	VSS_56	VSS_128	BF3
AJ20	VSS_57	VSS_129	BF48
AJ25	VSS_58	VSS_130	BF49
AJ27	VSS_59	VSS_131	BG17
AJ28	VSS_60	VSS_132	BG2
AJ30	VSS_61	VSS_133	BG22
AJ31	VSS_62	VSS_134	BG25
AK19	VSS_63	VSS_135	BG28
AK20	VSS_64	VSS_136	
AK25	VSS_65	VSS_137	
AK27	VSS_66	VSS_138	
AK28	VSS_67	VSS_139	
AK30	VSS_68	VSS_140	
AK31	VSS_69	VSS_141	
AK4	VSS_70	VSS_142	
AK46	VSS_71	VSS_143	
	VSS_72	VSS_144	

CNP-H_BGA874 Rev1.1

CNP-H

UH1L

BG3	VSS_145	VSS_196	M24
BG33	VSS_146	VSS_197	M32
BG37	VSS_147	VSS_198	M34
BG4	VSS_148	VSS_199	M49
BG46	VSS_149	VSS_200	M5
C12	VSS_150	VSS_201	N12
C25	VSS_151	VSS_202	N16
C30	VSS_152	VSS_203	N34
C4	VSS_153	VSS_204	N35
C48	VSS_154	VSS_205	N37
C5	VSS_155	VSS_206	N38
D12	VSS_156	VSS_207	P26
D16	VSS_157	VSS_208	P29
D17	VSS_158	VSS_209	P4
D30	VSS_159	VSS_210	P46
D33	VSS_160	VSS_211	R12
D6	VSS_161	VSS_212	R16
E10	VSS_162	VSS_213	R26
E13	VSS_163	VSS_214	R29
E15	VSS_164	VSS_215	R3
E17	VSS_165	VSS_216	R34
E19	VSS_166	VSS_217	R38
E22	VSS_167	VSS_218	R4
E24	VSS_168	VSS_219	T17
E26	VSS_169	VSS_220	T18
E31	VSS_170	VSS_221	T32
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E42	VSS_174	VSS_225	T7
E8	VSS_175	VSS_226	U12
F41	VSS_176	VSS_227	U15
F43	VSS_177	VSS_228	U17
F47	VSS_178	VSS_229	U21
G44	VSS_179	VSS_230	U24
G6	VSS_180	VSS_231	U33
H8	VSS_181	VSS_232	U38
J10	VSS_182	VSS_233	V20
J26	VSS_183	VSS_234	V22
J29	VSS_184	VSS_235	V4
J4	VSS_185	VSS_236	V46
J40	VSS_186	VSS_237	W25
J46	VSS_187	VSS_238	W27
J47	VSS_188	VSS_239	W28
J48	VSS_189	VSS_240	W30
J9	VSS_190	VSS_241	Y10
K11	VSS_191	VSS_242	Y12
K39	VSS_192	VSS_243	Y17
M16	VSS_193	VSS_244	Y33
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CNP-H_BGA874 Rev1.1

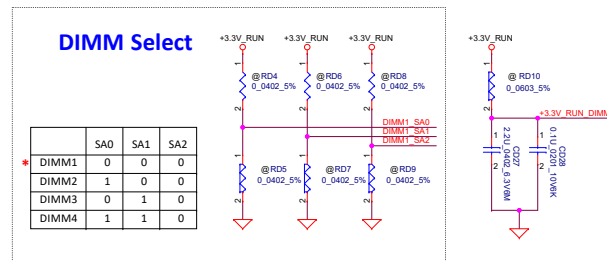
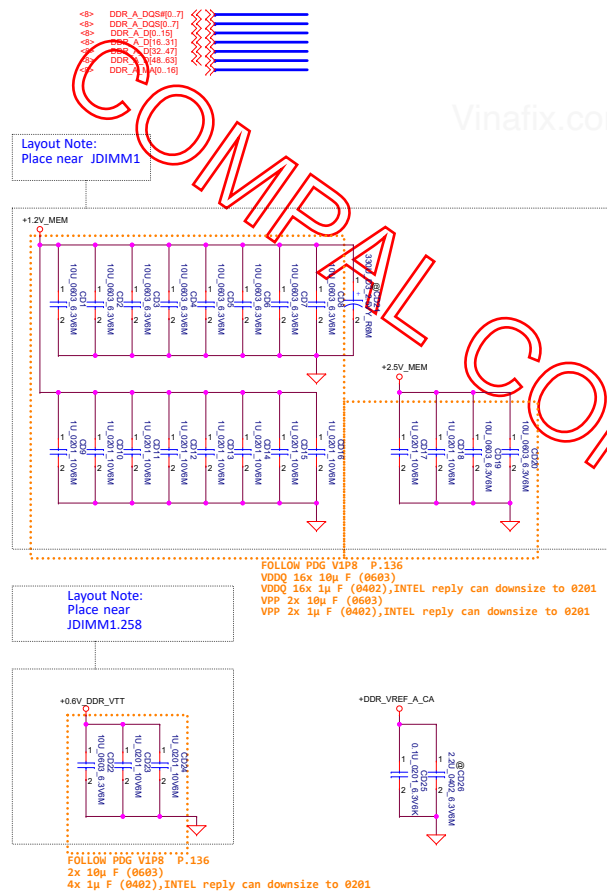
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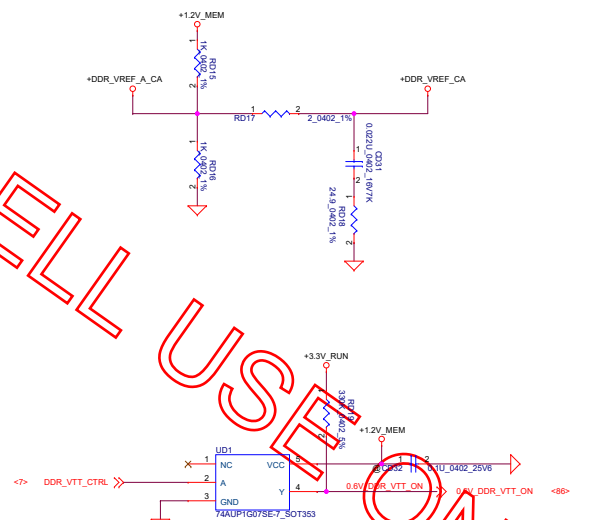
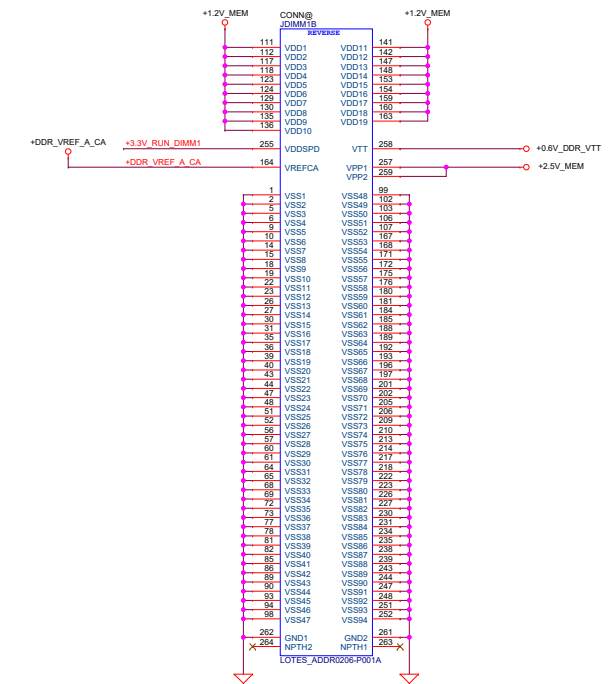
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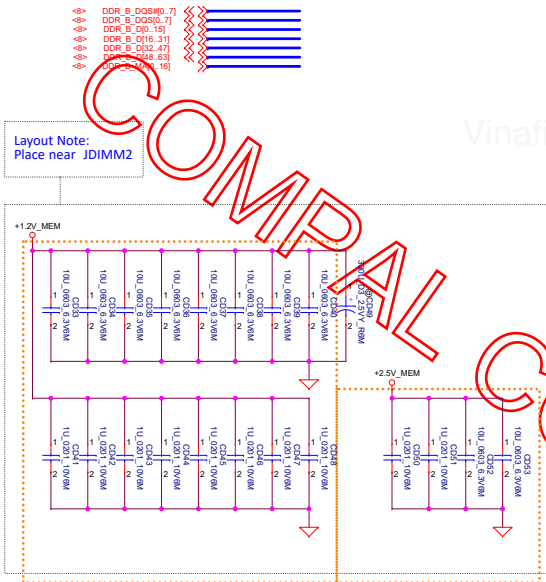
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Byte[1]	DQ[15:8]	DQS/DQS#[1]
Byte[2]	DQ[23:16]	DQS/DQS#[2]
Byte[3]	DQ[31:24]	DQS/DQS#[3]
Byte[4]	DQ[39:32]	DQS/DQS#[4]
Byte[5]	DQ[47:40]	DQS/DQS#[5]
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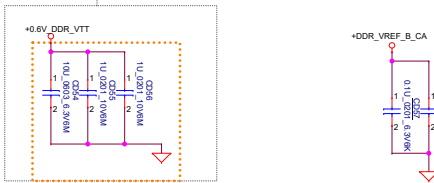


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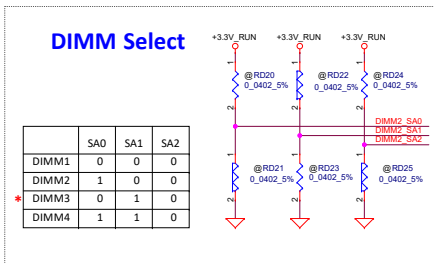


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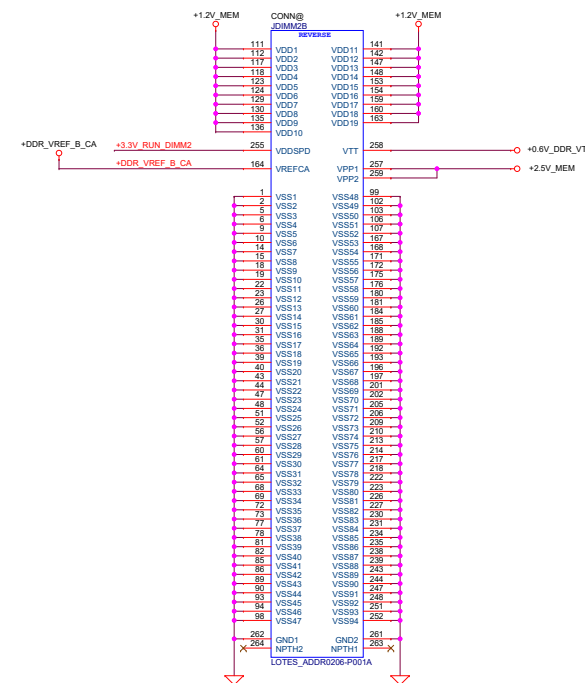
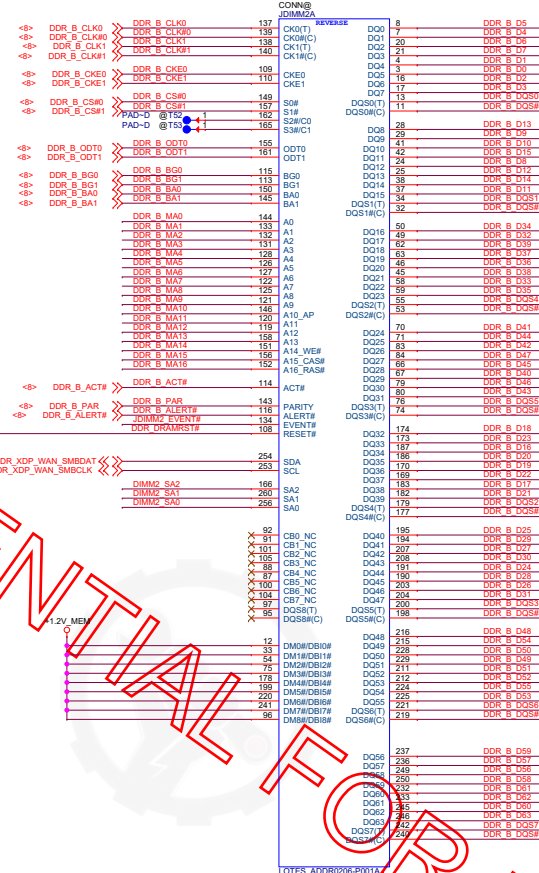
FOLLOW PDG V1P8 P.136
VDDQ 16x 10u F (0603)
VDDQ 16x 1u F (0402), INTEL reply can downsize to 0201
VPP 2x 10u F (0603)
VPP 2x 1u F (0402), INTEL reply can downsize to 0201



FOLLOW PDG V1P8 P.136
2x 10u F (0603)
4x 1u F (0402), INTEL reply can downsize to 0201



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Byte[3]	DQ[31:24]	DQS/DQS#[3]
Byte[4]	DQ[39:32]	DQS/DQS#[4]
Byte[5]	DQ[47:40]	DQS/DQS#[5]
Byte[6]	DQ[55:48]	DQS/DQS#[6]
Byte[7]	DQ[63:56]	DQS/DQS#[7]



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DP			
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LV601~LV605 link SM01000KR00 OK - 2017/03/16



Compal Electronics, Inc.

Title	<i>DP to HDMI2.0 & CONN</i>
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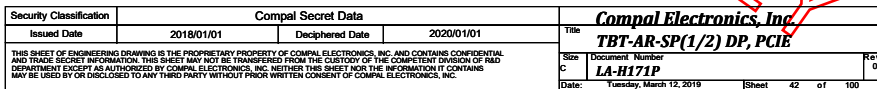
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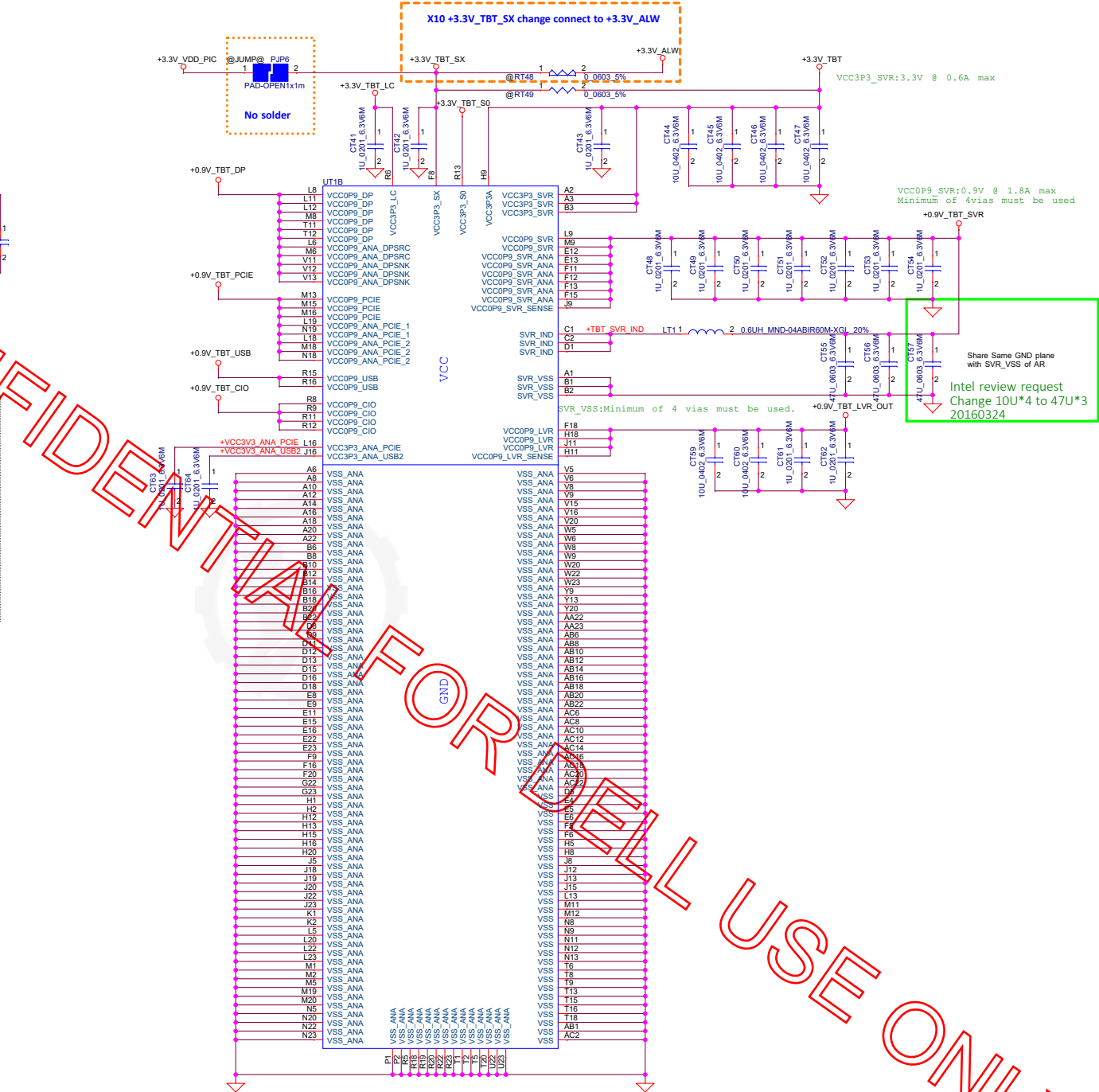
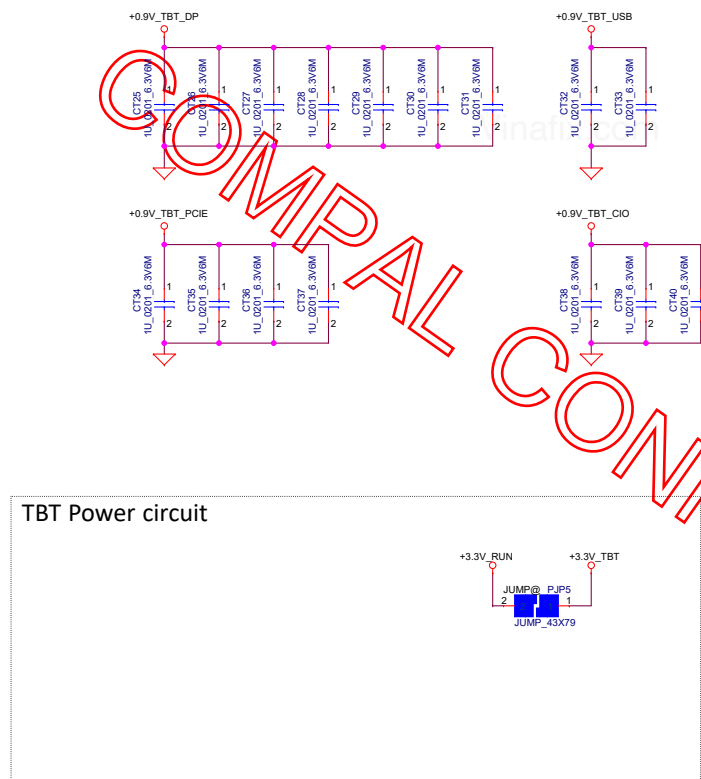


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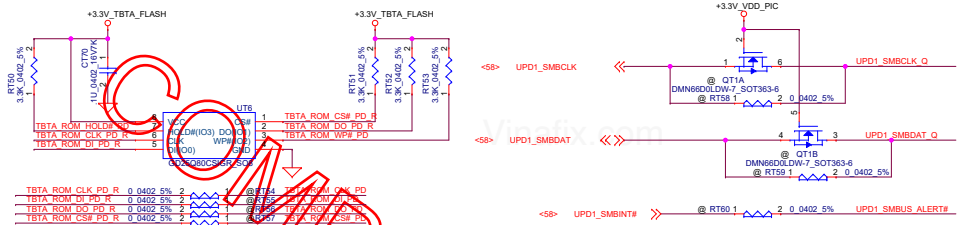




- ## Power Consumption

VCC3V3_S0_SYS	VCC3V3_TBT_SX	VCC3V3_1C	VCC3V3_ANA_PCIE	VCC3V3_ANA_USB2	
1.05A	0.19A	0.03A	0.1A	0.1A	
VCC0V9_SVR	VCC0V9_LVR_OUT	VCC0V9_DP	VCC0V9_PCIE	VCC0V9_USB	VCC0V9_CIO
1.83A	0.06A	0.7A	0.58A	0.22A	0.28A

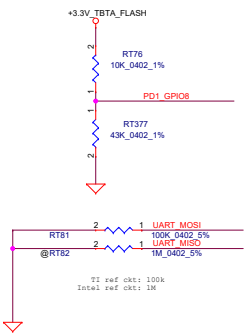
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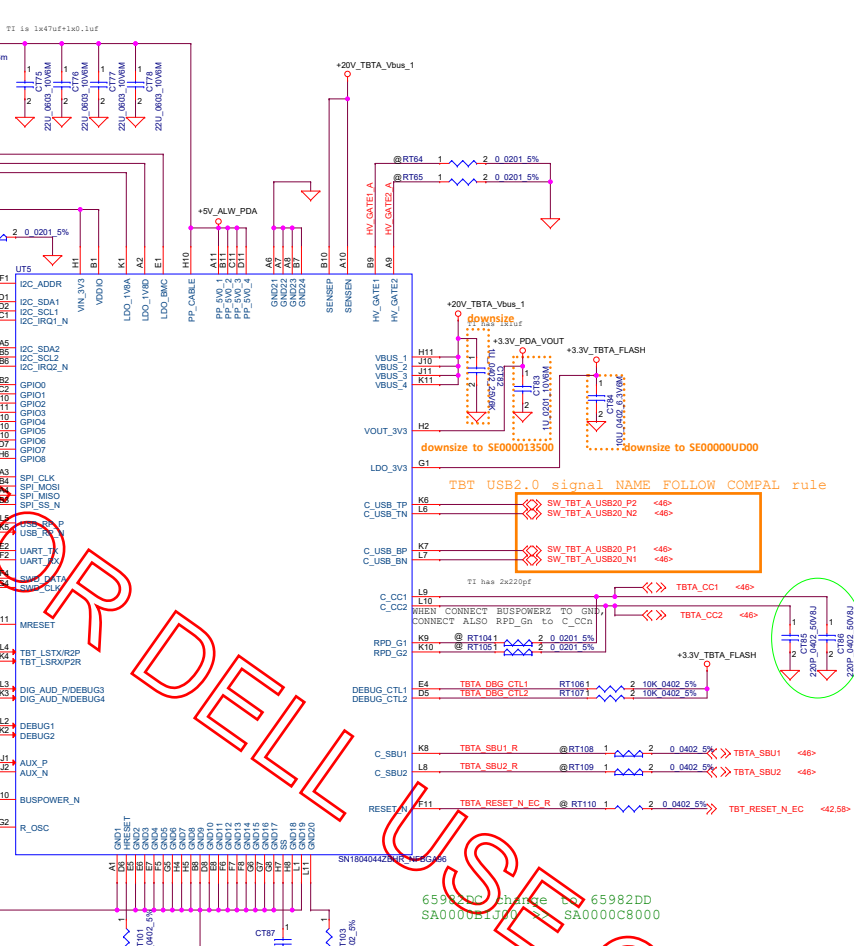
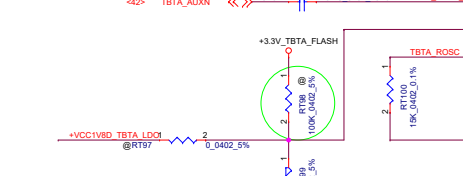
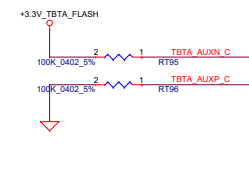
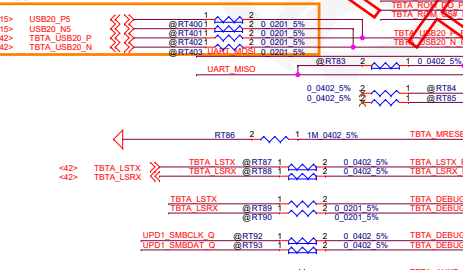
remove JDB1 9/6



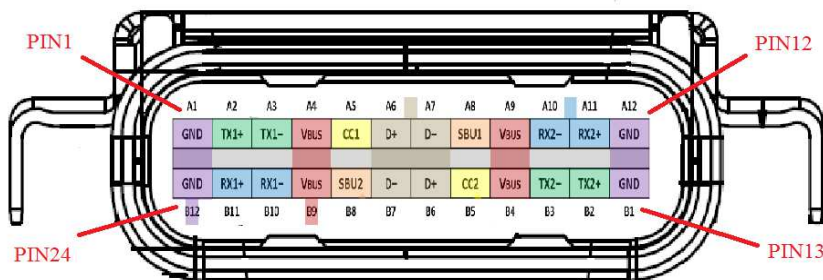
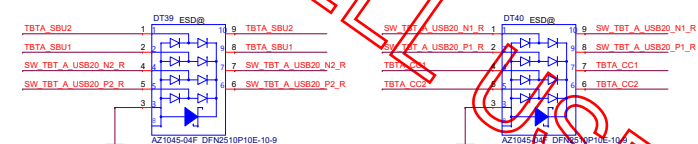
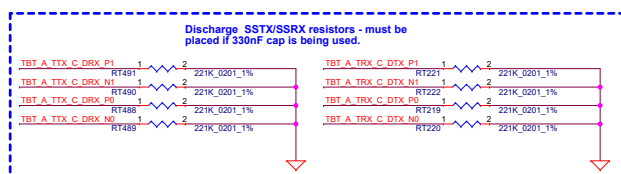
DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 - 3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 - 3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes - Sink, C and D pin configuration TI VID supported
0.20	0.28	2	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Sink, C and D pin configuration TI VID supported
0.40	0.48	4	DRP 5V @3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate.
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to DCP and can initiate.
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.



type c USB2.0 from PCH to PD



For AR Config



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TYPE-C Port2 (2/2)			
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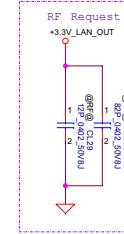
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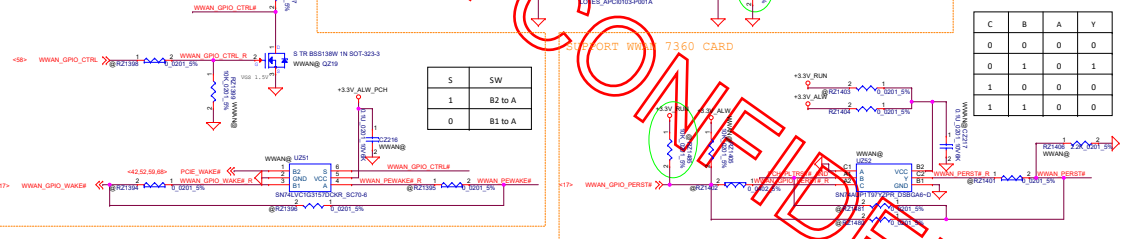
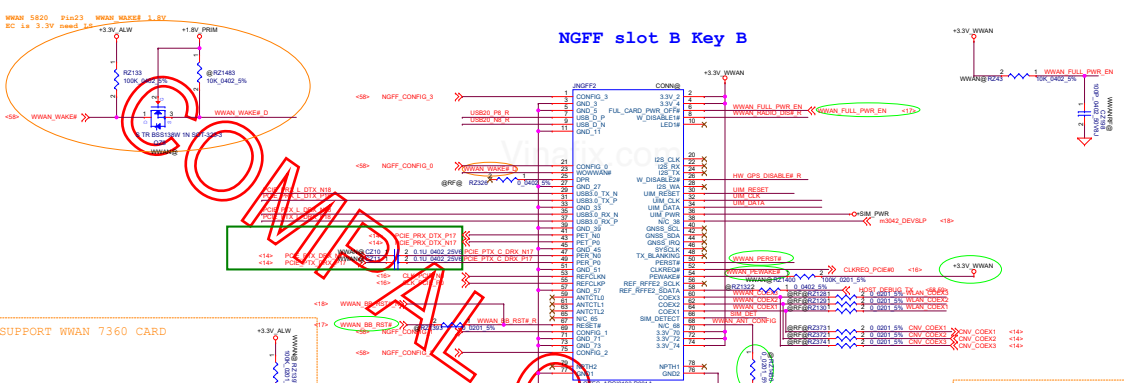
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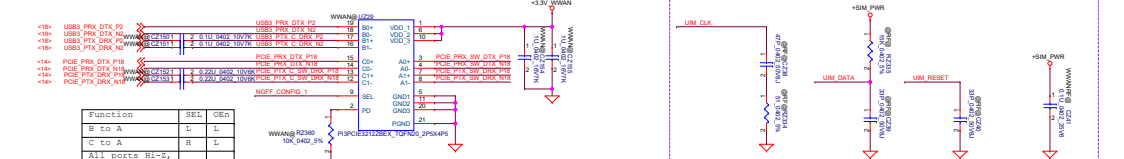
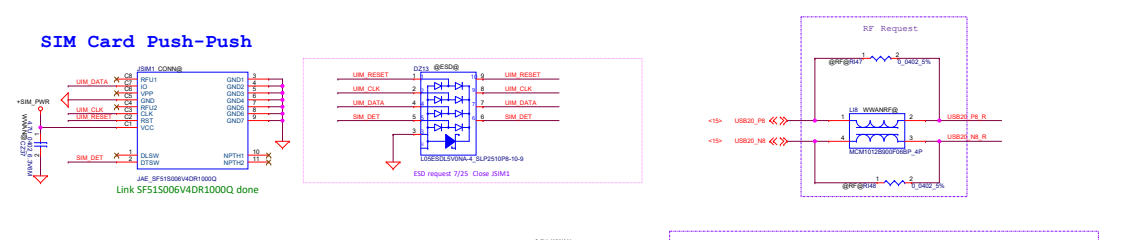
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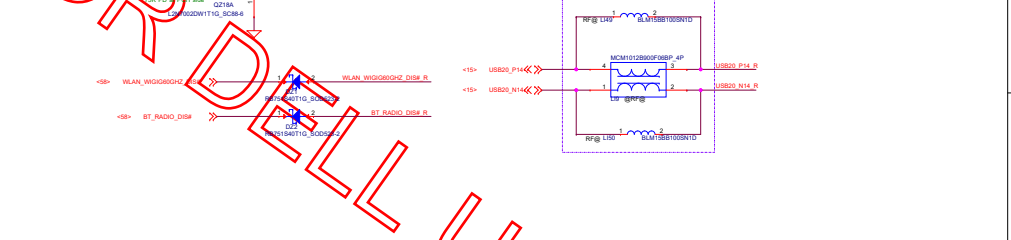
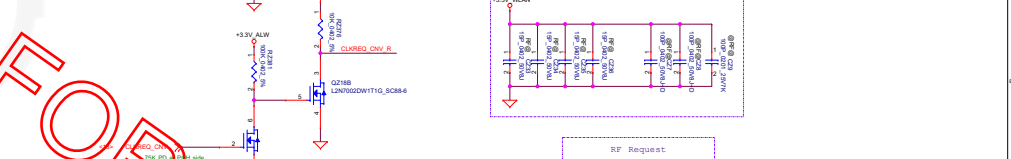
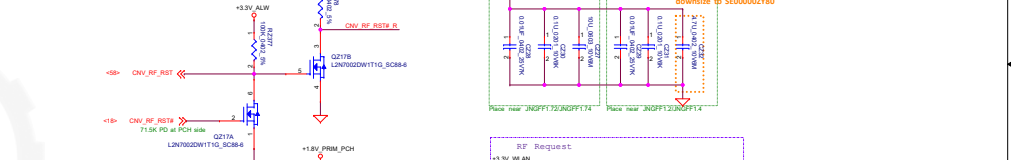
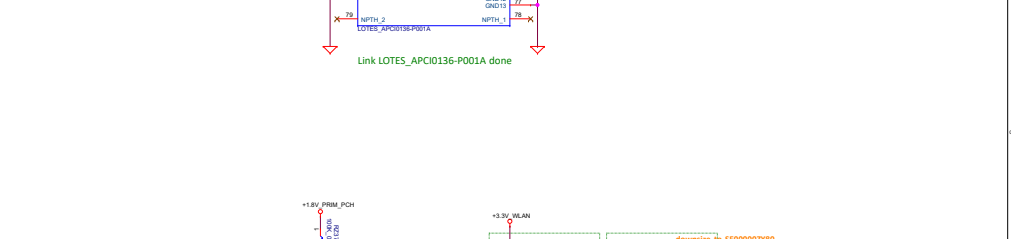
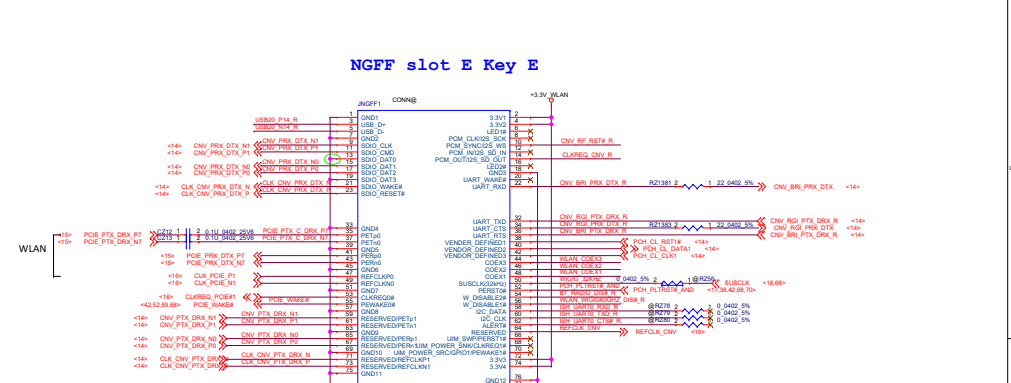
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				Drawn Number LA-H172P	
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STATE #	CONFIG_0 (PCE1)	CONFIG_1 (PCE2)	CONFIG_2 (PCE3)	CONFIG_3 (PCE4)	Module Type	m3042 PCIE# SATA
0	GND	GND (PEDET PD)	GND	GND (PEDET PD)	SSD-SATA	High
1	GND	GND (PEDET NC)	GND	GND (PEDET NC)	SSD-PCIE(2 lane)	Low
8	GND	GND (device NC)	HIGH (device NC)	HIGH (device NC)	WWAN	Low
	GND (device PD)	GND (device PD)	GND (device PD)	GND (device PD)	WWAN	Low
15	EC (MB PU)	EC (MB PU)	EC (MB PU)	EC (MB PU)	NA	Low



Function	SEL	GEN
RF to A	L	L
IC to A	H	L
All ports Hi-Z, IC power down	X	H



Security Classification	Compal Secret Data	2020/01/01	2020/01/01	2020/01/01	2020/01/01
Security Classification	2018/01/01	2018/01/01	2018/01/01	2018/01/01	2018/01/01
Security Classification	2018/01/01	2018/01/01	2018/01/01	2018/01/01	2018/01/01
Security Classification	2018/01/01	2018/01/01	2018/01/01	2018/01/01	2018/01/01
Security Classification	2018/01/01	2018/01/01	2018/01/01	2018/01/01	2018/01/01

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Title		WIGIG / WIDI
Size	Document Number	Rev 0.1
LA-H171P		
Date:	Friday, March 08, 2019	Sheet 53 of 100

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Title		
Reserve for PCIE device		
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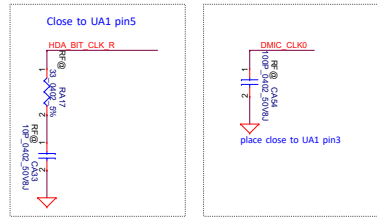
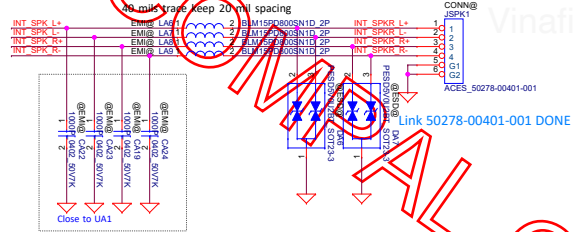
Title			
Reserve for PCIE device			
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BH audio codec SUPPORT ALC3204

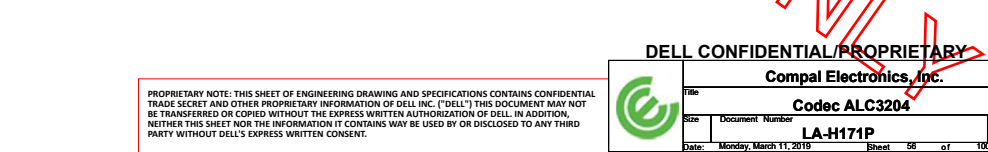
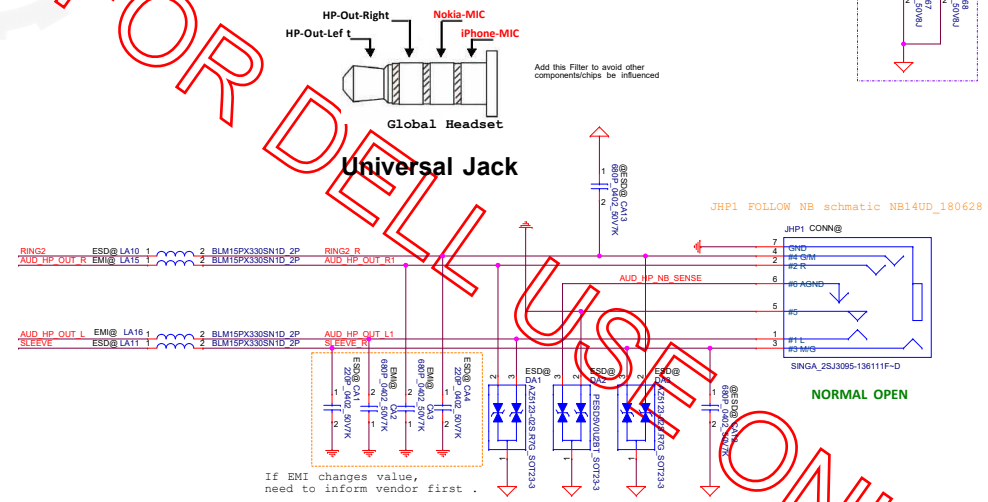
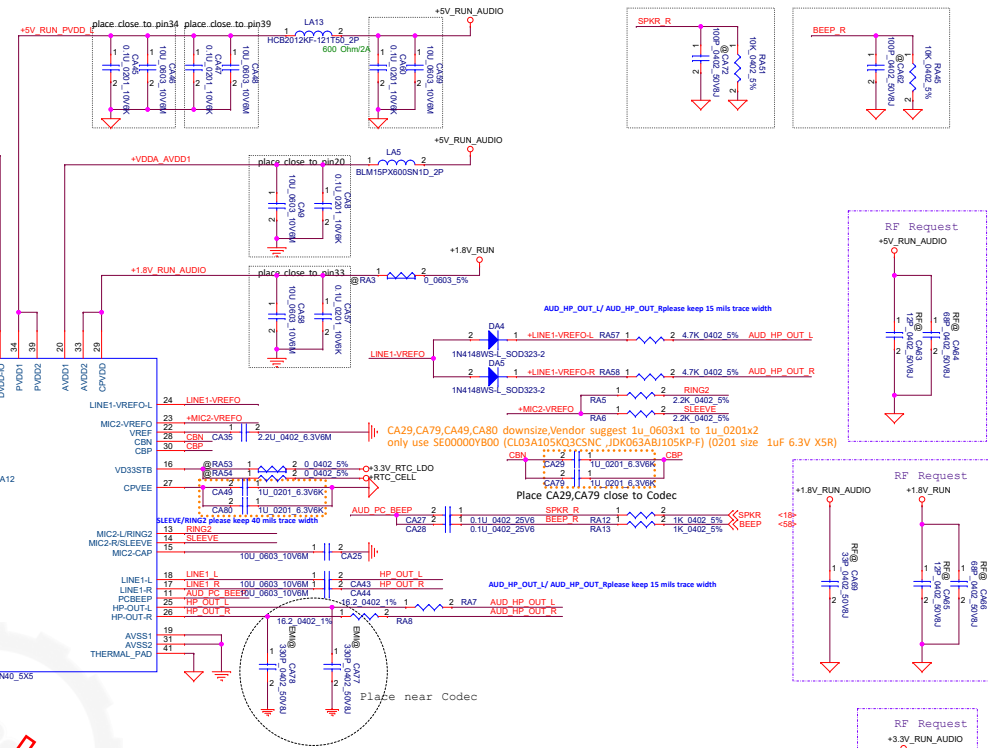
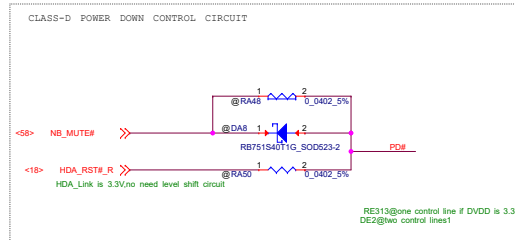
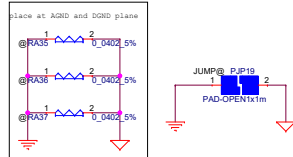
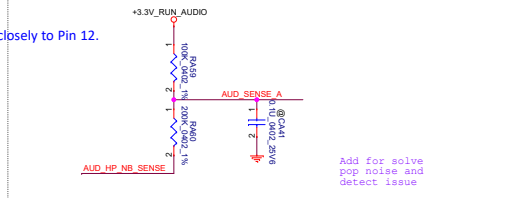
SCHMATIC FOLLOW NB15UD_180605

1W x 1ch, 4ohm (Transducer spec is 0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header



Place closely to Pin 12.



Vinafix.com

Reserve

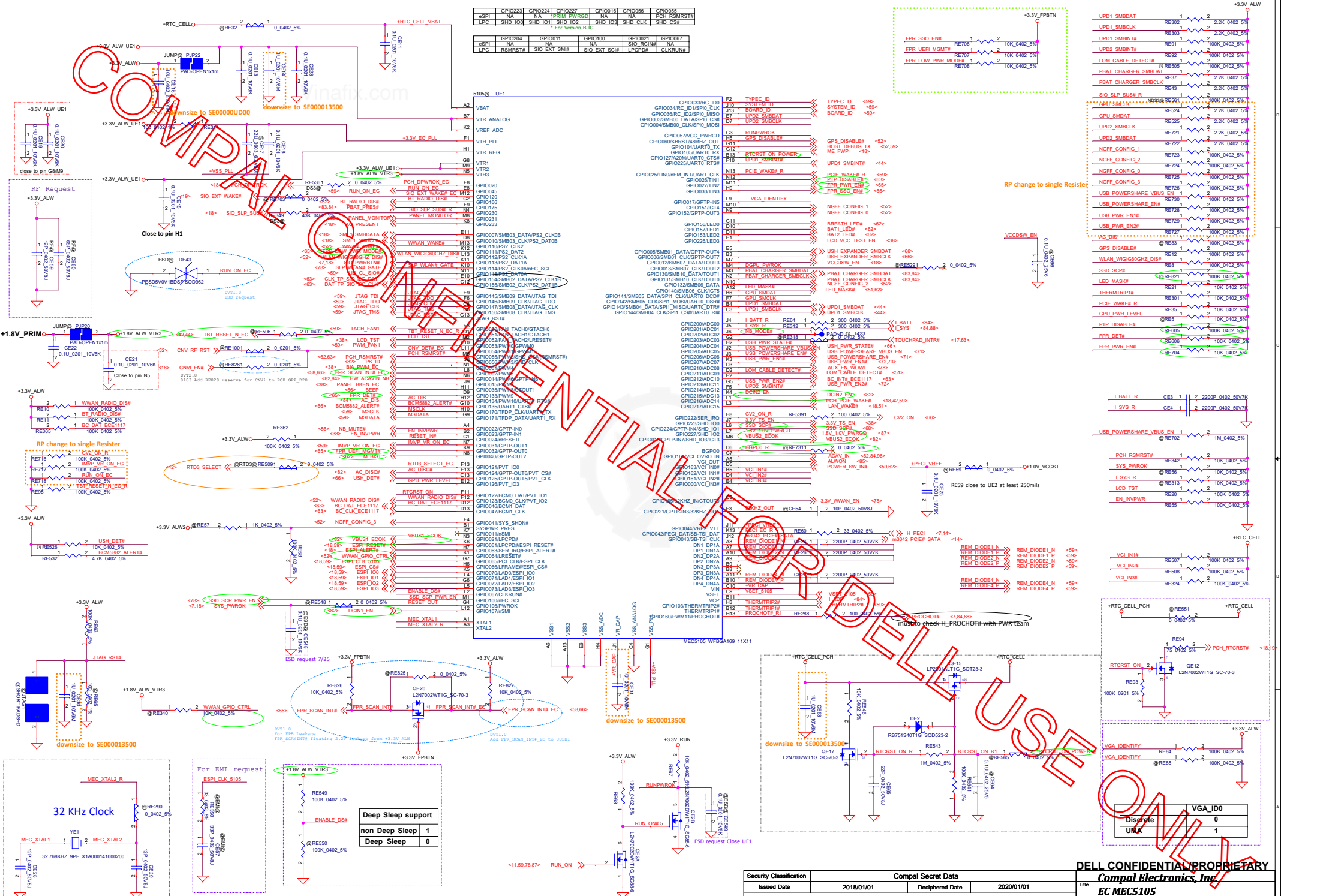
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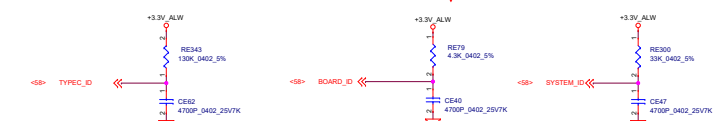
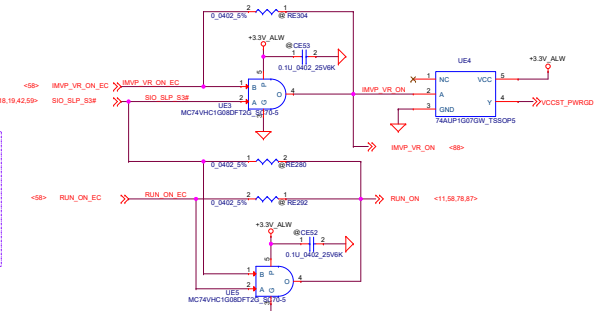
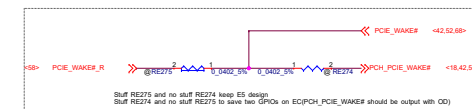
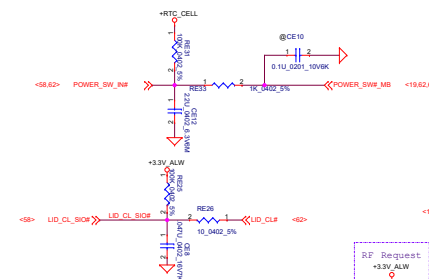
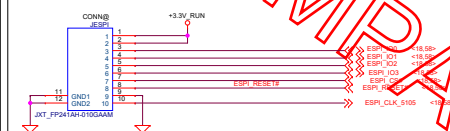
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Title			Rev 0.1
Audio Ampfilter			
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RE343	CE62	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	
2K	4700p	
1K	4700p	

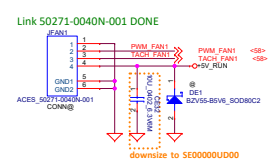
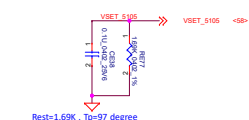
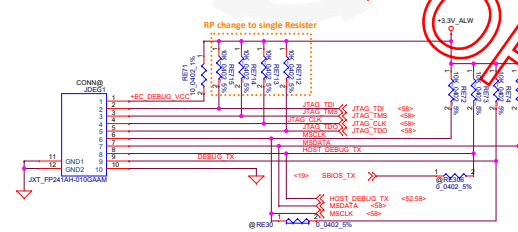
RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	
4.3K	4700p	A00
2K	4700p	
1K	4700p	

RE300	CE47	PANEL SIZE
240K	4700p	11"
130K	4700p	12"
62K	4700p	13"
33K	4700p	14"
8.2K	4700p	BR15 H
4.3K	4700p	17"
2K	4700p	BR15 P
1K	4700p	

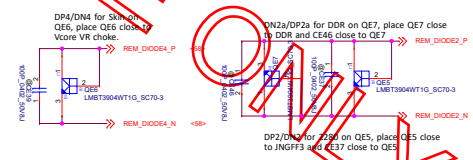
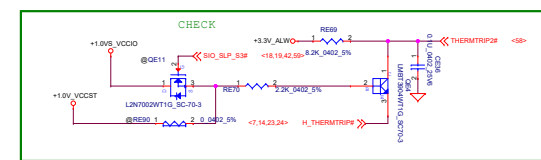
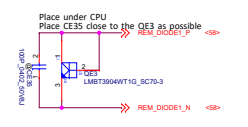
PD ACE_DET# rise t1 mel's meas u edf o m5 %68 %

BOARD_ID rise t1 mel's meas u edf o m5 %68 %

PANEL_ID rise t1 mel's meas u edf o m5 %68 %



5105 Channel	Locat i on
DP1/DN1	CPU (QE3)
DP2/DN2	2280 (QE5)
DN2a/DN2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)



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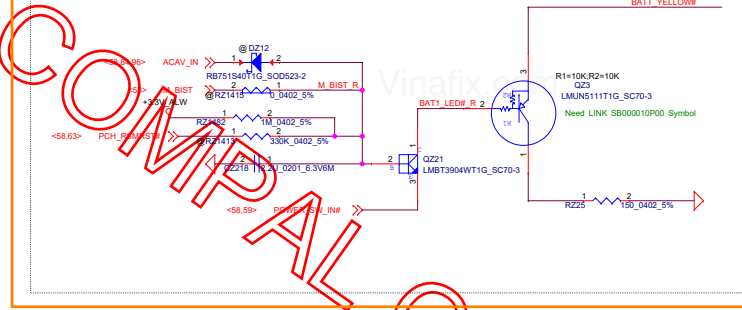
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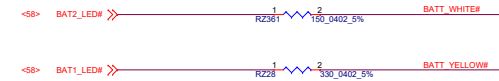
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Title		Secure & Reset IC	
Size	Document Number		Rev
	LA-H171P		0.1
Date:	Friday, March 08, 2019		Sheet 60 of 100

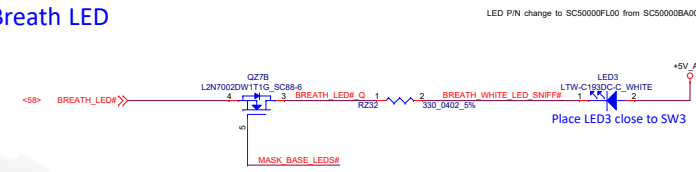
M BIST



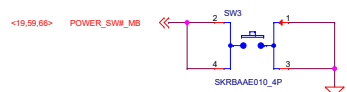
Bat tery LED



Breath LED



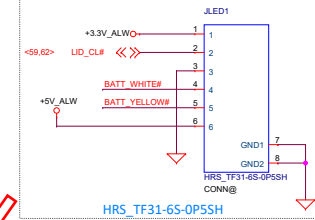
POWER & INSTANT ON SWITCH



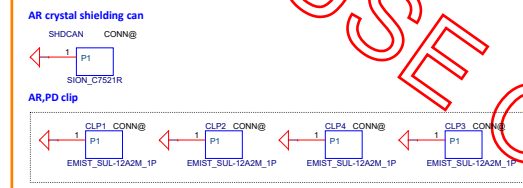
LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

FOLLOW NB schematic NB14UD_180605

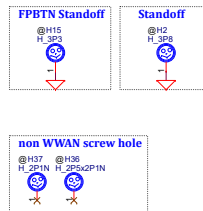
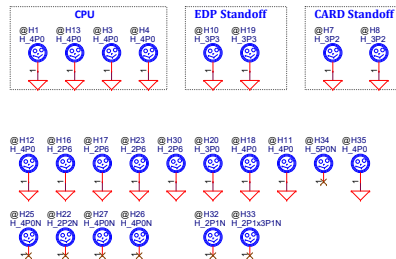
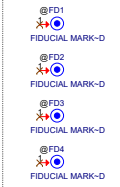
LED board CONN



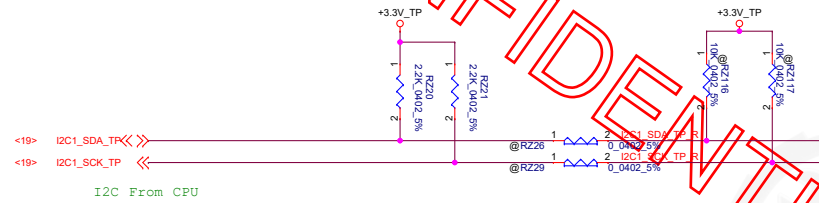
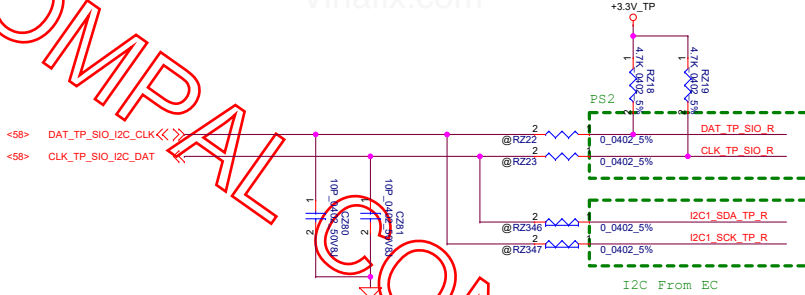
FOLLOW NB schematic NB15UD_180605



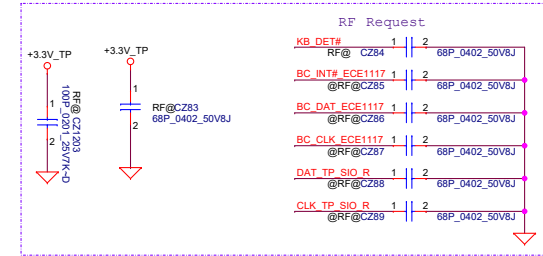
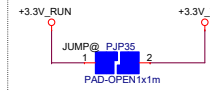
Fiducial Mark



Touch Pad

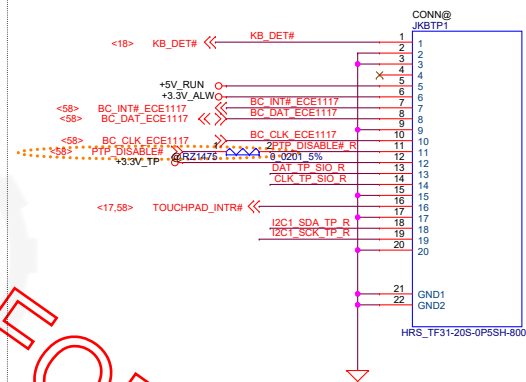


Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues

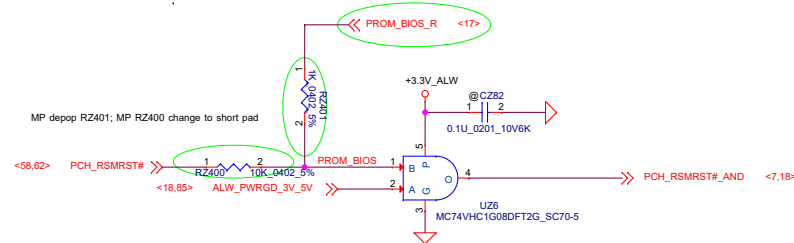


JKBTP1 FOLLOW NB schematic NB15UD_180628

Keyboard



RSMRST circuit



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Keyboard

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Title			
Reserve for KB/TP/LED/LID			
Size	Document Number		Rev
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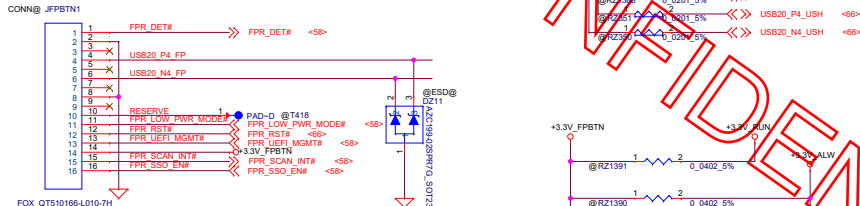
BH SUPPORT FPR in Power BUTTON SCHEMATIC FOLLOW NB15UD_180605

Vinafix.com

FP in PWR BUTTON connector

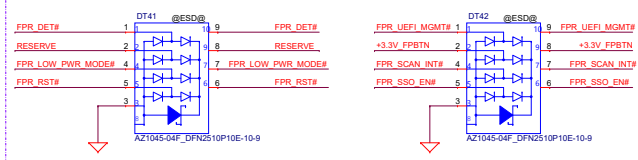
FP IN RTN USB2.0 need check port map

NEED check EC GPIO TABLE

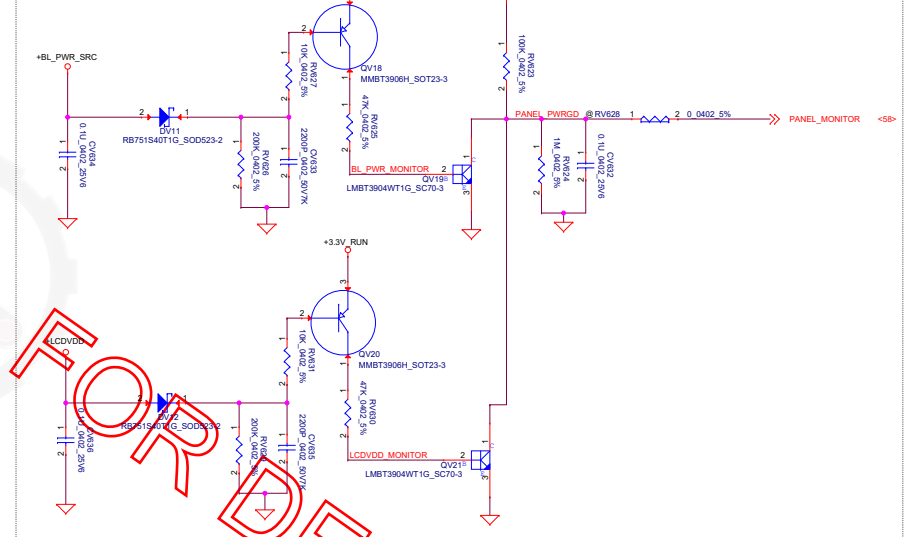


Compal MB CONN Symbol	Signal	FPR Symbol
2	GND	1
4	USB DP(D+)	2
6	USB DM(D-)	3
8	GND	4
10	RESERVED	5
12	FP RESET#	6
14	+3.3V_FPBTN	7
16	FPR_SSO_EN#	8
9	FPR_SCAN_INT#	9
13	FPR_UEFI_MGMT#	10
11	FPR_LOW_PWR_MODE#	11
12	NA	12
7	NA	13
5	NA	14
3	NA	15
1	FPR_DET#(GND)	16

9/26 ESD Request



For BL_PWR_SRC & LCDVDD monitor



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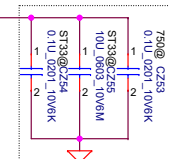
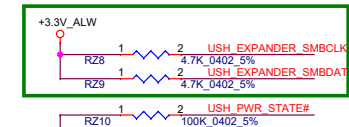
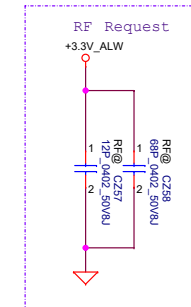
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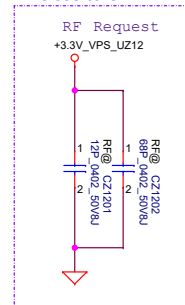
Title	Document Number	Rev
FP in PWRBTN	LA-H172P	0.1
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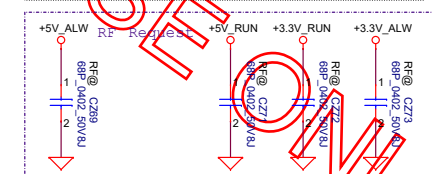
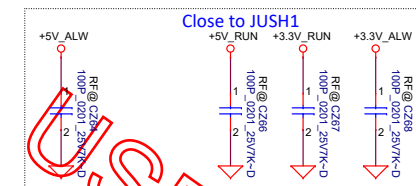
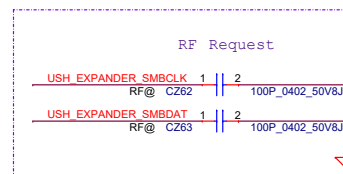
BH USH/B SUPPORT CV3
SCHEMATIC FOLLOW NB15UD_180605



For NPTC750
Depop RZ112, RZ1408
Pop RZ1407, RZ1409, R



(REMOVE ~~CZ6~~



JUSH1 FOLLOW NB schmatic NB15UD 180628

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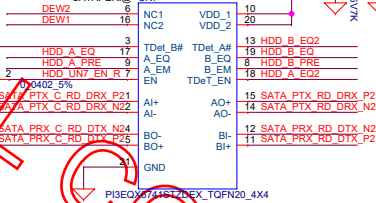
USH & TPM

Title		USH & TPM	
Size	Document Number	Rev	
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	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC	TDet_EN
TI	GN1	DEW1	GND	DEW1	GND
Parade	GN1	REXT	B_EQ2	DEW	A_EQ2

SATA Repeater

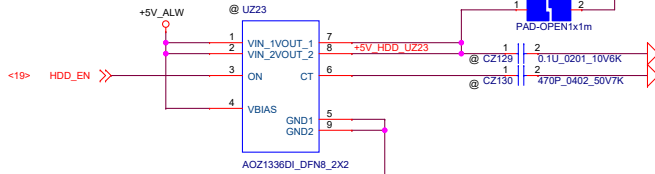


		HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN19	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
Pericom	PI3EQX6741ST	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC	NC	PD (RN7)	PD (RN9)
TI	SN75LVCP601	PD (RN11)	NC	PD (RN21)	PD (RN19)	NC (IFU)	NC (IFU)	PD (RN6)	PH (RN8)
Parade	PS8527C	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC (1/2 VDD)	NC (1/2 VDD)	PD (RN15)	NC (1/2 VDD)

			A_EQ	B_EQ		A_EM	B_EM	
Main	Pericom	0	3dB	3dB	0	0dB	0dB	
		NC	6dB	6dB	NC			
		1	9dB	9dB	1	1.5dB	1.5dB	
2nd	TI	0	7dB	7dB	0	0dB	0dB	
		NC	0dB	0dB	NC	-4dB	-4dB	
		1	14dB	14dB	1	-2dB	-2dB	
3rd	Parade	EQ2	EQ1	A_EQ	B_EQ		A_EM	B_EM
		(M = VDD/2)						
		0	M	2.4dB	2.4dB	0 M 1	0dB -3.5dB -6dB	0dB -3.5dB -6dB
		0	0	7.4dB	7.4dB			
		0	1	14.4dB	14.4dB			
		M	M	12.2dB	12.2dB			
		M	0	9.4dB	9.4dB			
		M	1	13.3dB	13.3dB			
		1	M	6.2dB	6.2dB			
		1	0	11.2dB	11.2dB			
		1	1	5dB	5dB			

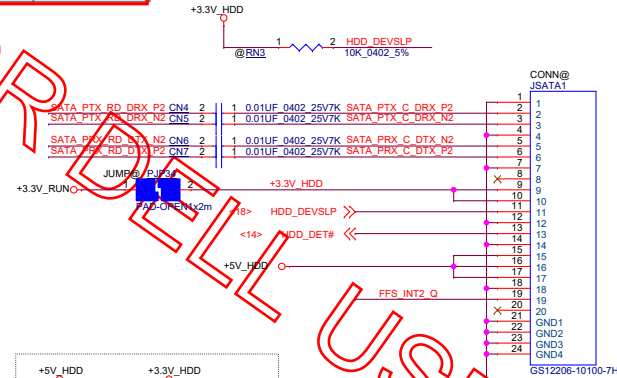
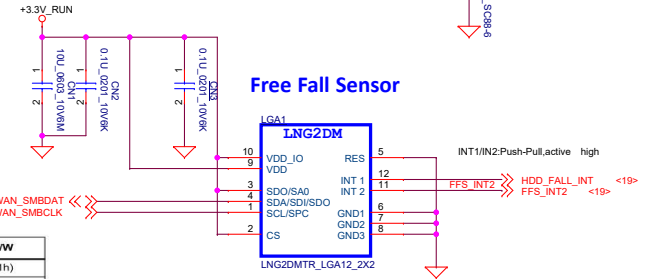
* red color is current setting

+5V_HDD source



Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

Free Fall Sensor



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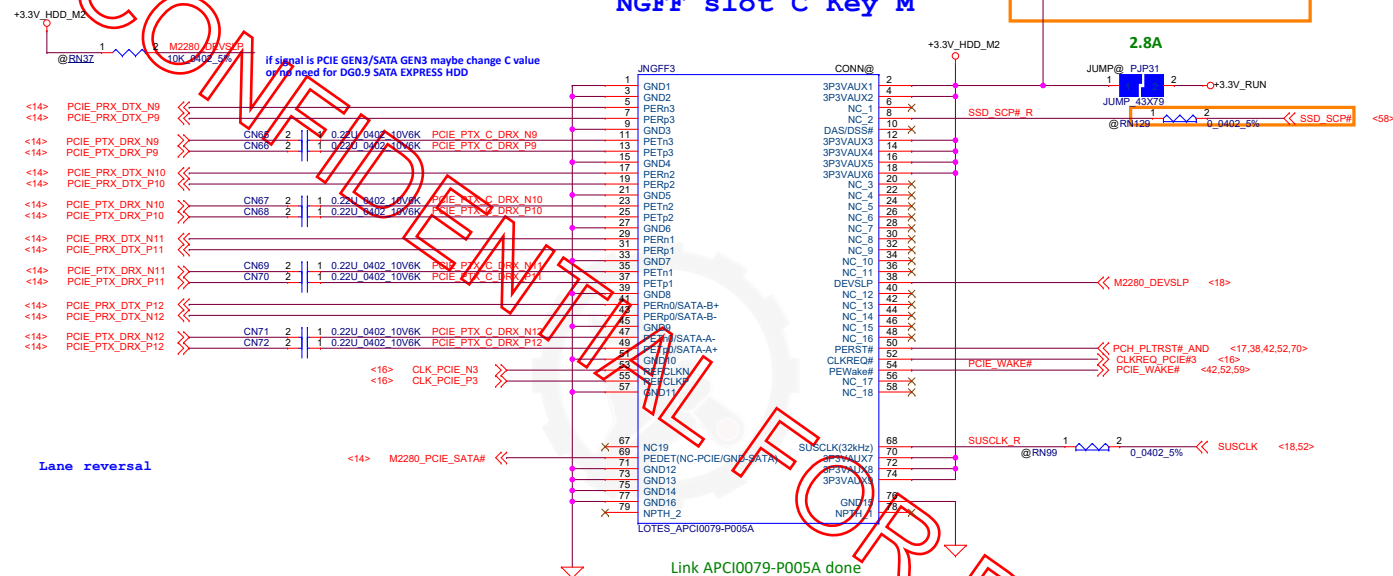
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HDD CONN

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[illegible]

NGFF slot C Key M



Link APCI0079-P005A done

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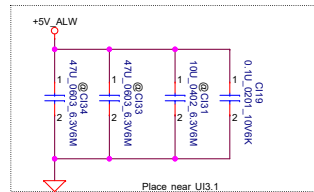
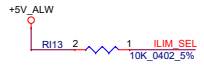
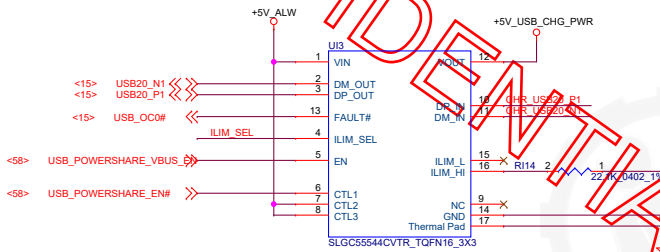
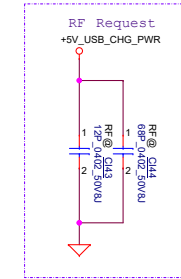
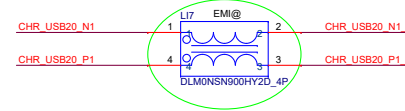
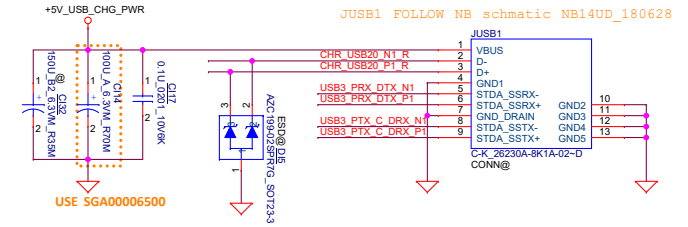
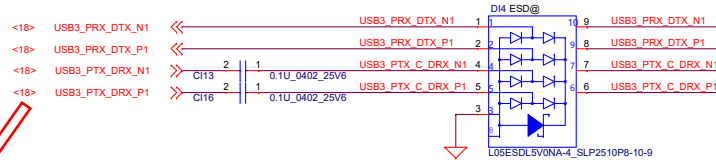


Card Reader

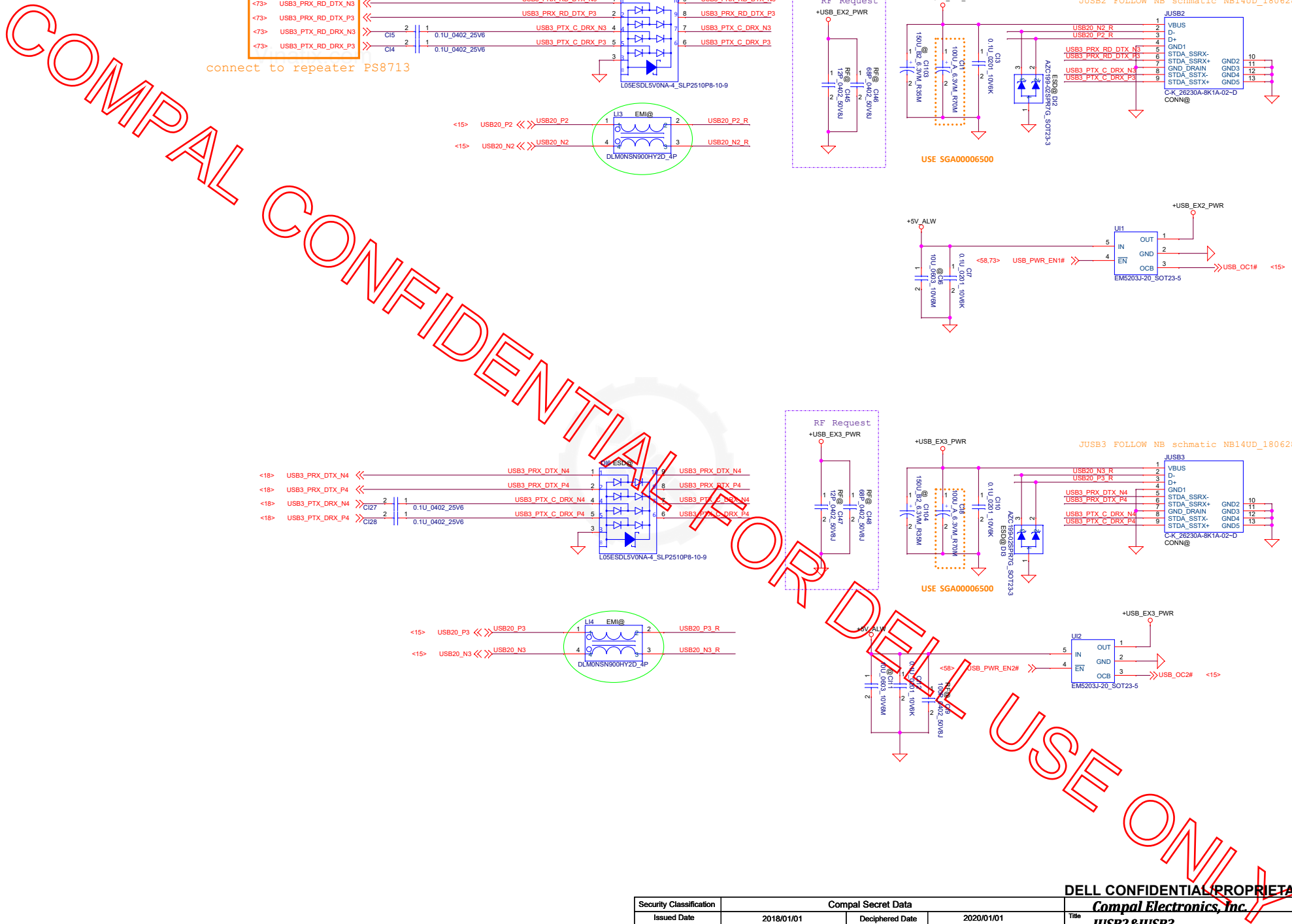
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For PWR SW + Charger combine IC

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USB SW					
Size		Document Number		Rev	
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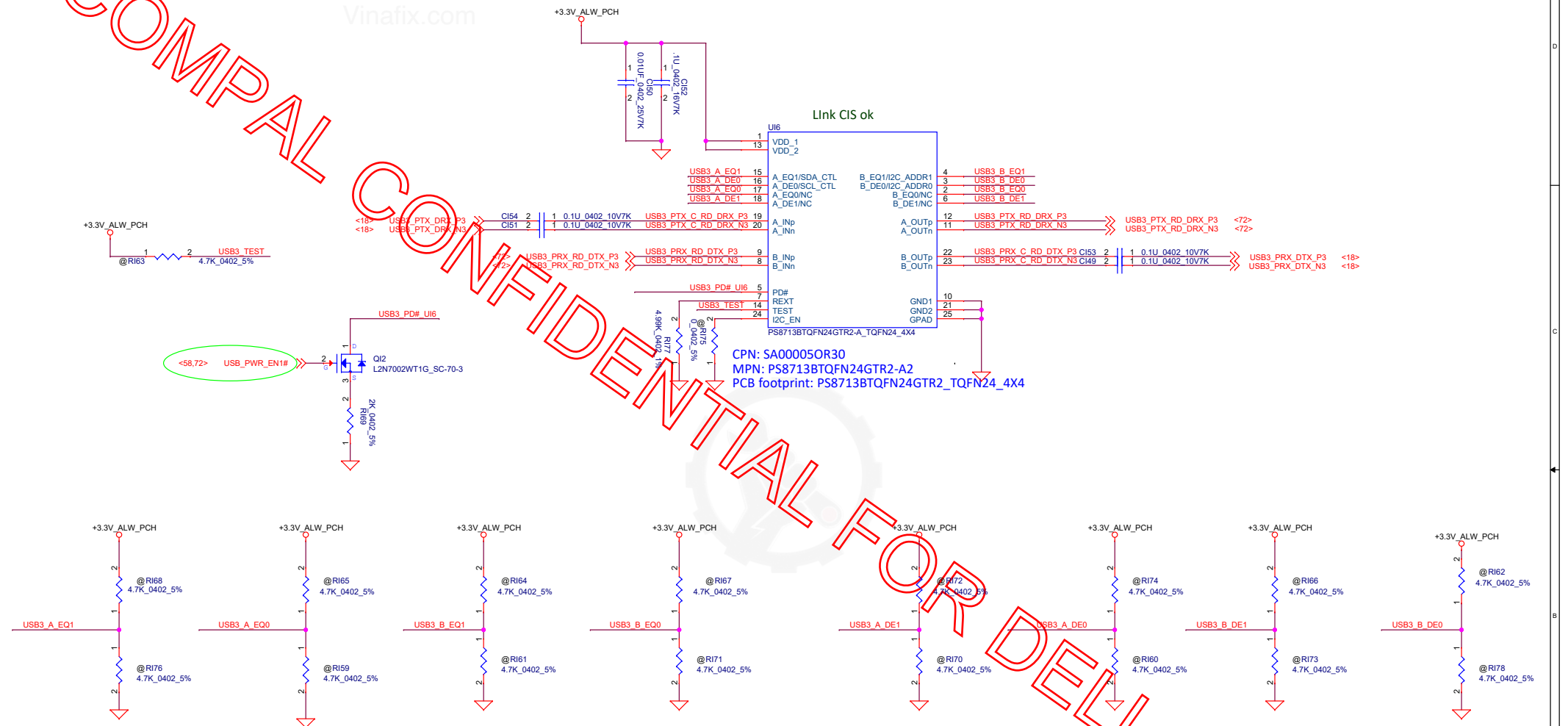


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Title		JUSB2&JUSB3			
Size	Document Number		Rev		0.1
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BH USB3.0 add repeater PS8713
SCHMATIC FOLLOW BRMLK14UD_20180316 P.47

FOR LEFT JUSB2 USE

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Parade_PS8713B

A_EQ1	A_EQ0	B_EQ1	B_EQ0	Recommended EQ	A_DE1	A_DE0	B_DE1	B_DE0	Recommended DE
0	0	0	0	loss up to 9.5dB	0	0	0	0	3.5dB de-emphasis
0	1	0	1	loss up to 13dB	0	1	0	1	No de-emphasis
1	0	1	0	loss up to 4.5dB	1	0	1	0	2.7dB de-emphasis
1	1	1	1	loss up to 7.5dB	1	1	1	1	5dB de-emphasis

Both A_EQ&B_EQ have internal pull-down 150k

Both A_DE&B_DE have internal pull-down 150k

Security Classification

Compal Secret Data

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USB3.0 Repeater for JUSB3

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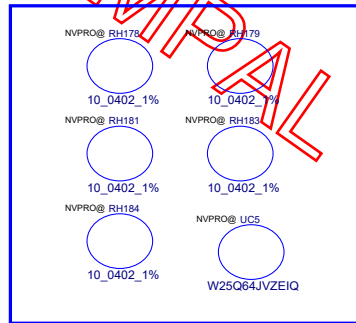


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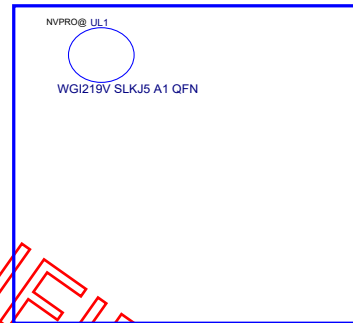
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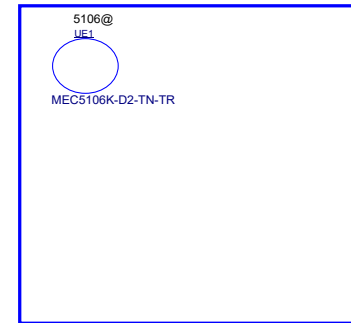
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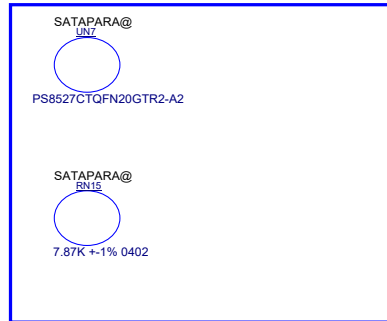
FOR NVPRO LAN chip BOM OPTION



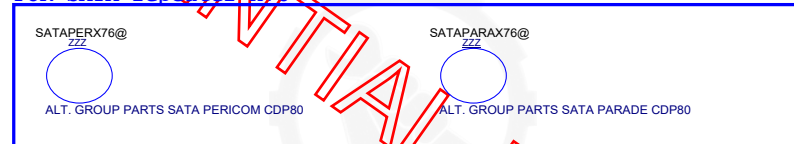
FOR EC MEC5106 BOM OPTION



FOR SATA repeater BOM OPTION



FOR SATA repeater X76



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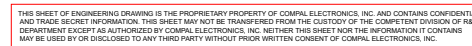
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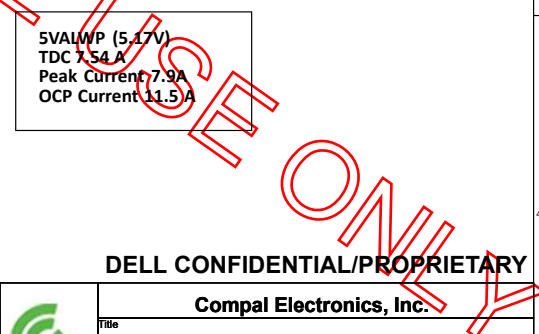
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DB-2283P

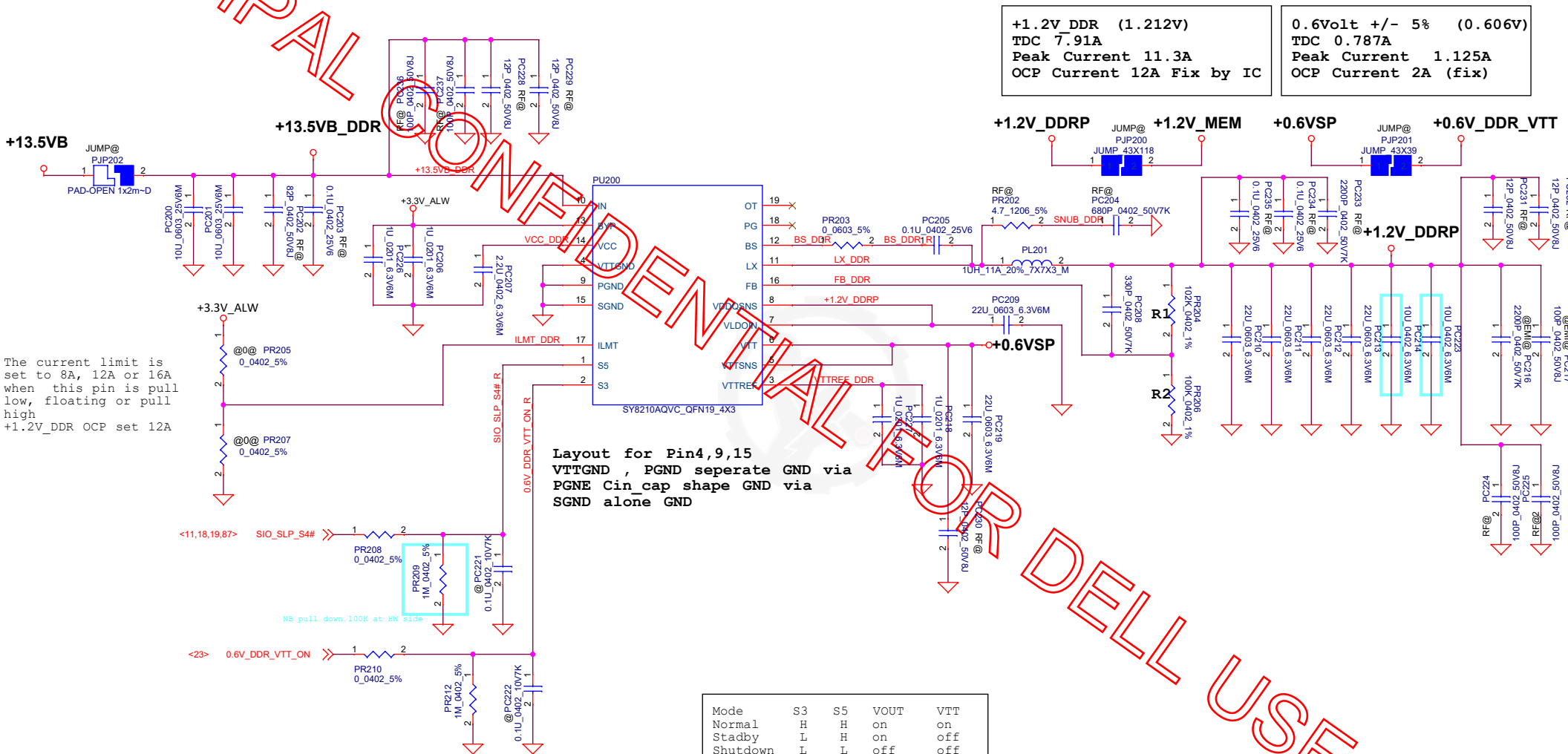
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+1.2V DDR (1.212V) TDC 7.91A Peak Current 11.3A OCF Current 12A Fix by IC	0.6Volt +/- 5% (0.606V) TDC 0.787A Peak Current 1.125A OCF Current 2A (fix)
--	--

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high
+1.2V_DDR OCP set 12A

Layout for Pin4,9,15
VTTGND , PGND separte GND via
PGNE Cin_cap shape GND via
SGND alone GND

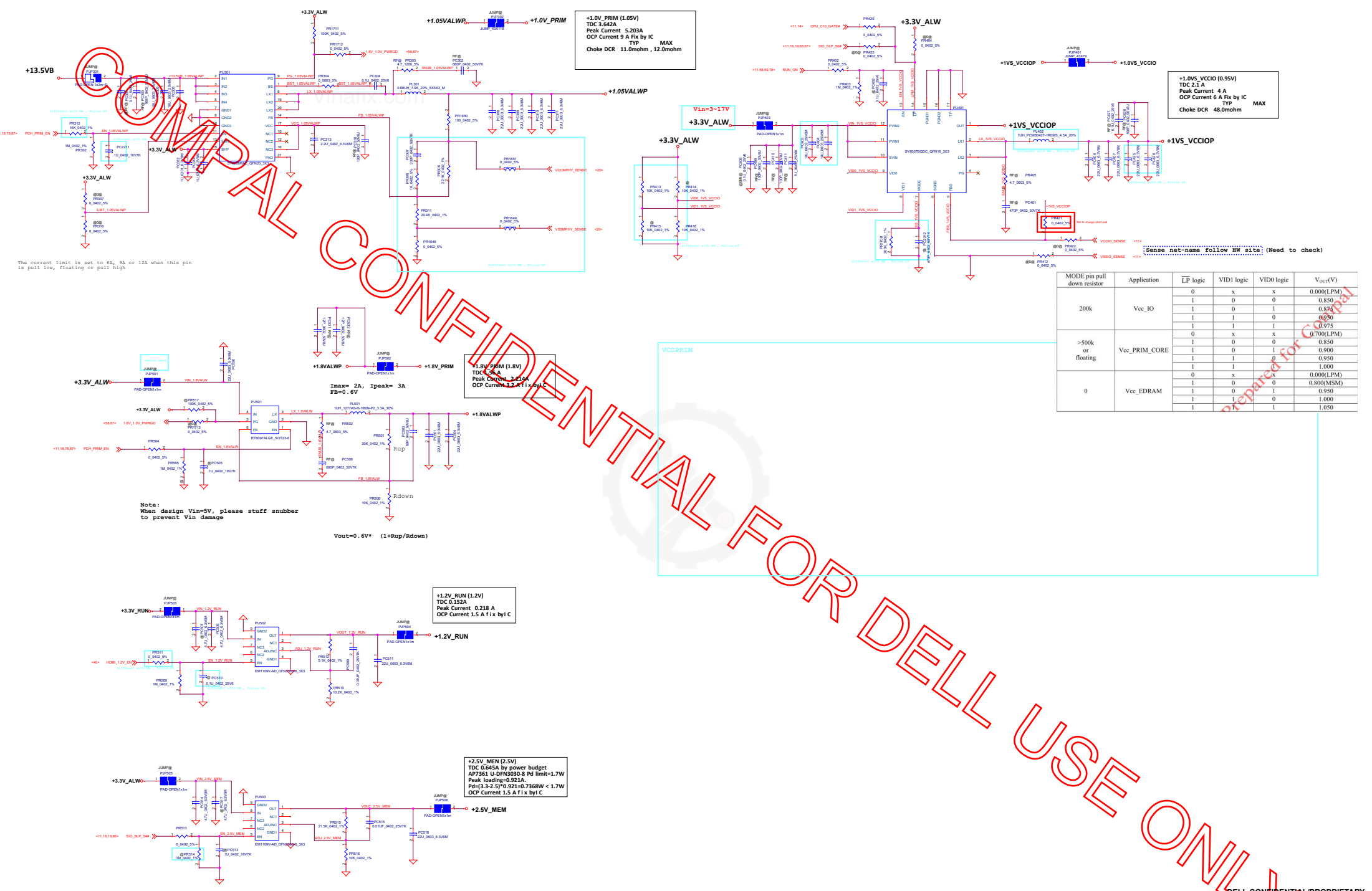
Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

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+1.2V MEN/+0.6V_DDR_VTT			
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The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

+1.0V_PRIM (1.05V)
TDC 3.642A
Peak Current 9 A Fix by IC
TYP MAX
Choke DCR 11.0mohm, 12.0mohm

+1.8V_PRIM (1.8V)
TDC 3.6A
Peak Current 3.21A
OCF Current 1.5 A Fix by IC

+1.2V_RUN (1.2V)
TDC 0.152A
Peak Current 0.218 A
OCF Current 1.5 A Fix by IC

+2.5V_MEM (2.5V)
TDC 0.645A by power budget
AP7361 U-DPM300-8 Pd limit=1.7W
Peak loading=0.521A
Pd=(3.3-2.5)*0.921=0.7368W < 1.7W
OCF Current 1.5 A Fix by IC

+1.0V_VCCIO (0.95V)
TDC 2.1A
Peak Current 4 A
OCF Current 6 A Fix by IC
TYP MAX
Choke DCR 48.0mohm

MODE pin pull down resistor	Application	LP logic	VID1 logic	VID0 logic	V _{OUT} (V)
200k	V _{CC} _JO	0	x	x	0.000(LPM)
		1	0	0	0.850
		1	0	1	0.950
		1	1	1	0.975
>500k or floating	V _{CC} _PRIM_CORE	0	x	x	0.700(LPM)
		1	0	0	0.850
		1	0	1	0.900
		1	1	0	0.950
0	V _{CC} _EDRAM	0	x	x	0.000(LPM)
		1	0	0	0.800(MSM)
		1	0	1	0.950
		1	1	0	1.000
		1		1	1.050

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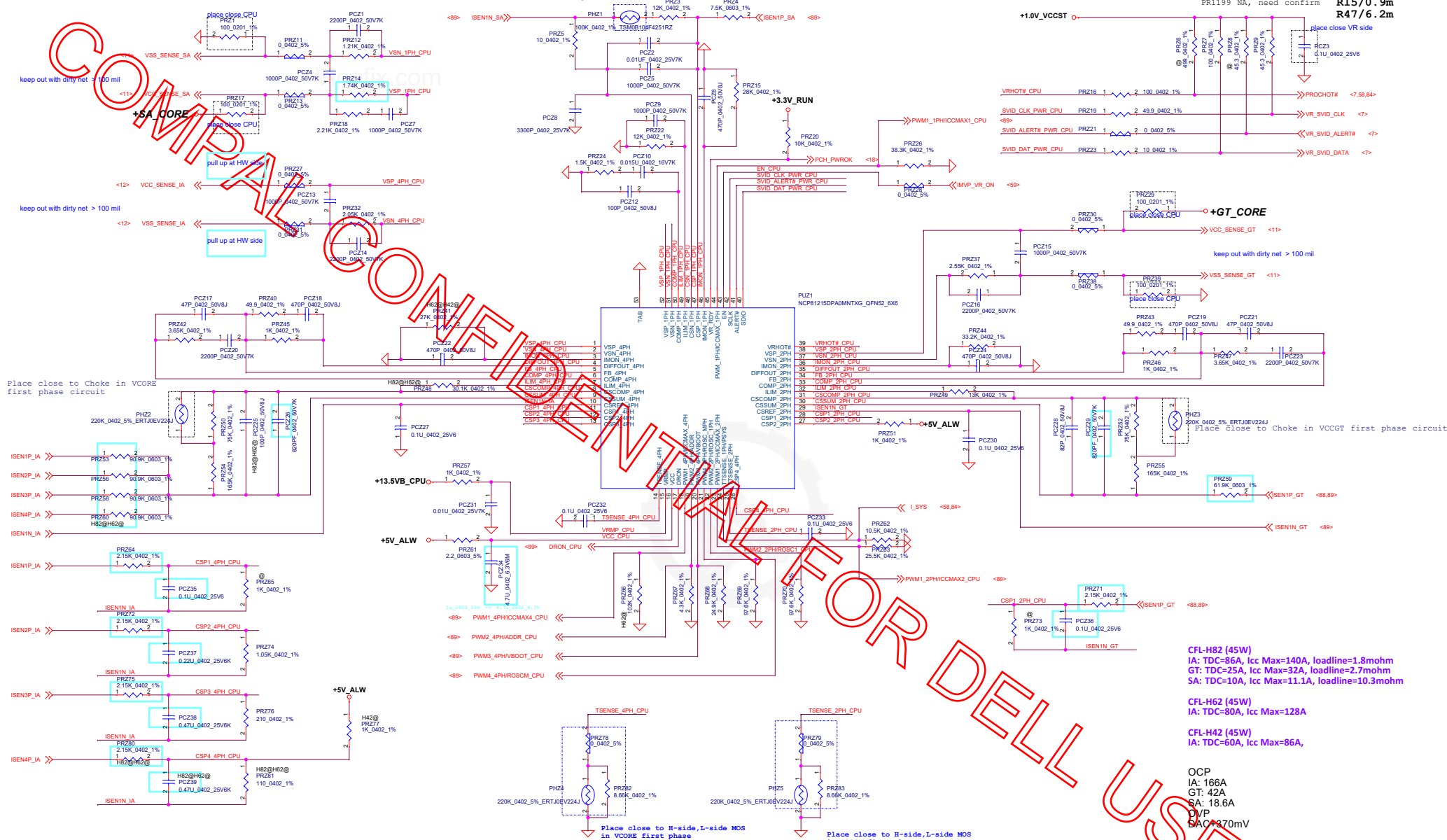
Layout need to be clean.
PHZ1 close to SA choke
PHZ1.1, PRZ2.2, PRZ4.2 differential to IC

TSM0B224J4702RE
7.2329K@105C
R15/0.9m
R47/6.2m

Place close to Choke in VCCSA first phase circuit

PR1199 NA, need confirm

place close VR side



CFI-H82 (45W)
IA: TDC=86A, Icc Max=140A, loadline=1.8mohm
GT: TDC=25A, Icc Max=32A, loadline=2.7mohm
SA: TDC=10A, Icc Max=11.1A, loadline=10.3mohm

CFI-H62 (45W)
IA: TDC=80A, Icc Max=128A

CFI-H42 (45W)
IA: TDC=60A, Icc Max=86A,

OCV
IA: 166A
GT: 42A
SA: 18.6A
OVP
DAC=370mV

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CPU CORE

DB-2283P

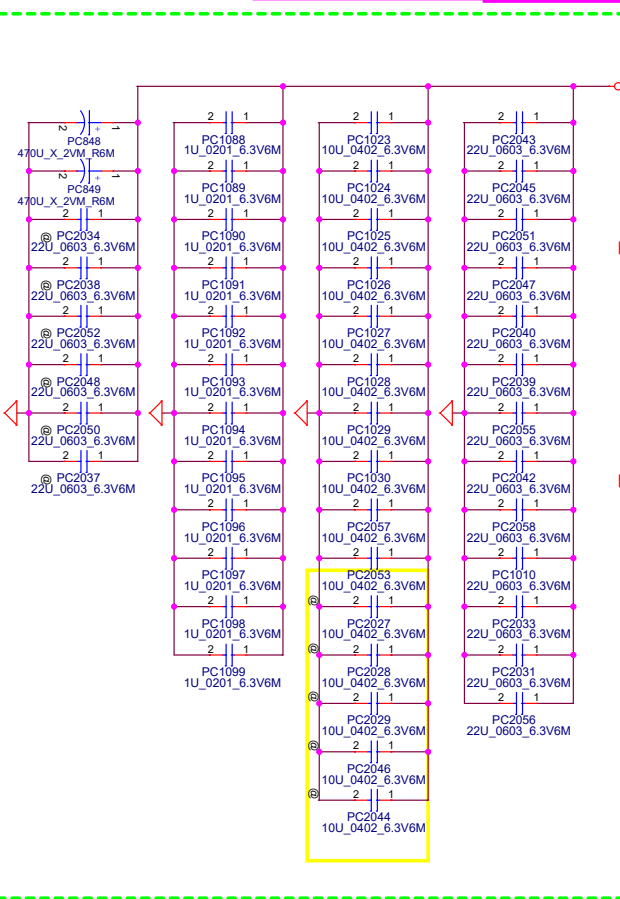
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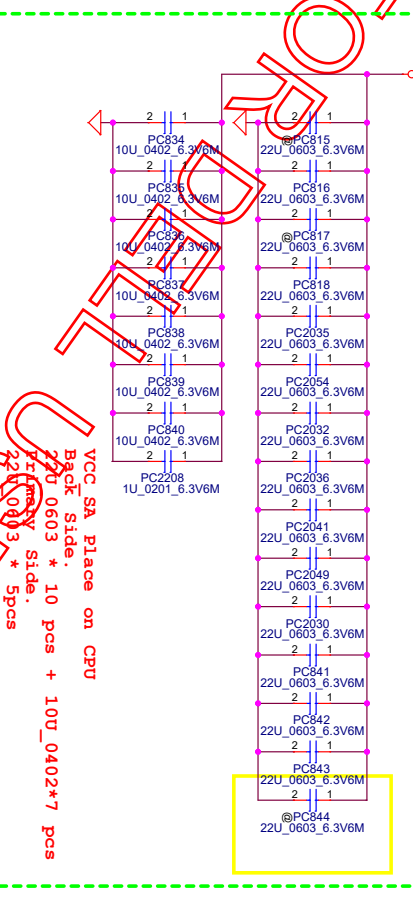
+IA_CORE



+GT_CORE



+SA_CORE



+IA_CORE		H62		H82	
caps(uF)	size	Backside	Primary	Backside	Primary
47	0603			1	7
22	0603		23	22	9(DV)
10	0402		21	21	
1	0201		24	48	
220	D7	2		2	
330	D2		2		2

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CPU Decoupling Cap

Document Number: DB-2283P


Date: 11/05/1993

Rev: 0.1

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CPU

H82@ PR24T 24.3K_0402_1%
H42@ PR24T 68.1K_0402_1%
H42@ PR248 20.5K_0402_1%
H82@ PR268 110K_0402_1%




OUTPUT CAPS


H82@ PC1034 47U_0603_6.3V6M



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Issue Description		Solution Description	
item	Title	Description	Remark
1	change 0 Ohm to Short pad:	<p>UMA(55): PR19,PR20,PR22,PR25,PR861,PR42,PR44,PR46,PR47,PR49,PR104,PR105,PR119,P R120,PR709,PR713,PR715,PR719,PR721,PR722,PR727,PR729,PR731,PR736,PR73 7,PR740,PR741,PR743,PR814,PR816,PR818,PR820,PR826,PR827,PR829,PR1652, PR836,PR840,PR844,PR853,PR854,PR858,PR859,PRZ11,PRZ13,PRZ27,PRZ31,PRZ 78,PRZ79,PRZ30,PRZ38,PRZ21,PRZ28,PR1651,PR1649</p> <p>DIS(4): PR1302,PR1305,PR1315,PR1406</p> <p>add note : Not to change short pad PR866,PR114 PR1616,PR1618,PR1620,PR1626,PR1624,PR1622, PR1617,PR1619,PR1621,PR1627,PR1625,PR1623</p>	
2	Power path S1 fast turn off circuit simplify	un stuff PC13,PU3,PR45,PC814,PU801,PR855	Follow NB
3	+3.3V_VDD_DCIN LDO circuit	<p>change PR871 and PR872 to 22_0805_5% (SD002220A80) Function field 39.10 PD803 Pin 1 add net name : +20V_LDO_input ✖Please check layout trace at least 20 mil Delete PR868 colay footprint</p>	Follow NB
4	Charger UVP and CPU OVP circuit modify	<p>PR3010 change value from 14.7K to 147K(SD034147380) PR3011 change value from 4.32K to 43.2K(SD034432280)</p> <p>Change PU3000 from SA0000A6500 to SA0000A6400</p>	<p>Follow NB,for more sequence margin.</p> <p>SA0000A6500 test has abnormal problem when default initial</p>
5	Common BOM modify	Change PLH1,PLH2,PLH3,PLH4,PLT1,PL1302,PL1301 from SH00001D800 to SH00001EE00	change to common PN
6	Dr.mos Main/2nd/3rd source is group alternative, need to place on same layer for SMT process.	<p>Change PR1616,PR1618,PR1620,PR1626,PR1624,PR1622 from 0_0402 to 0_0201 Change PR1617,PR1619,PR1621,PR1627,PR1625,PR1623 from 0_0402 to 0_0201</p>	Placement need modify the x76 components on the same layer
7	Fine tune GPU enable sequence	Change PR1309 from 100K_0402_1% to 1K_0402_1% (SD034100180)	EE requirements Fine turn GPU Power sequence
<div> <div>  <div> <div>DELL CONFIDENTIAL/PROPRIETARY</div> <div>Compal Electronics, Inc.</div> <div>PWR P.I.R</div> </div> </div> <div> <div>Size</div> <div>Document Number</div> <div>Date: Friday, March 08, 2019</div> </div> <div> <div>Rev</div> <div>0.1</div> <div>Sheet 101 of 101</div> </div> </div>			
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1	70	2018/05/23	follow BH ARD (v0.5) define	JSD1 connector use Micro SD type,QR1.3 change to gnd	0.1 (X00)
2	44	2018/05/23	PD USB2.0 source from PCH follow X10 NB	PD USB2.0 source change from TBT to PCH depop RT402,403 pop RT400,RT401	0.1 (X00)
3	46	2018/06/05	add TBT type c short protection circuit	implement AR type c short protection circuit ,add RT190~RT197,CT326~CT329,CT95~CT98,RT488~RT491,RT219~RT222	0.1 (X00)
4	43	2018/06/05	change PD and AR power rail	1.PJP6 no solder,RT48 pop 2.add RT399 pop,RT398 depop for +3.3V_VDD_PIC option 3.add RT482 depop,RT483 pop for +3.3V_VDD_PIC_PDA option,remove PJP7	0.1 (X00)
5	38	2018/06/05	follow NB JEDP1,JTS1 pin define	remove LV27,DV4,JIR1,UH1.M6,UH1.N8 add JIRTS1,pin define follow NB add RV733,RV732 JEDP1.1 +5V_TSP- +TS_PWR_SRC JEDP1.2 USB20_N9_R- NC JEDP1.3 USB20_P9_R- NC QV8.1 +5V_TSP- +TS_PWR_SRC check TS_INT#,TS_I2C_SDA,TS_I2C_SCL GPIO	0.1 (X00)
6	11	2018/06/08	power follow compal naming rule,HW synchronize change net name	VSS_IO_SENSE- VSSIO_SENSE VCC_IO_SENSE- VCCIO_SENSE VSS_GT_SENSE- VSS_SENSE_GT VCC_GT_SENSE- VCC_SENSE_GT VCC_SA_SENSE- VCC_SENSE_SA VSS_SA_SENSE- VSS_SENSE_SA VCC_SENSE- VCC_SENSE_IA VSS_SENSE- VSS_SENSE_IA +PWR_SRC- +13.5VB +TBTA_Vbus_1- +20V_TBTA_Vbus_1	0.1 (X00)
7	56	2018/06/08	change audio codec solution to ALC 3204	follow ARD implement ALC 3204 schmatic(UA1)	0.1 (X00)
8	66	2018/06/08	follow USH/B pin define	JUSH1 pin define follow NB,support USH/B CV3 remove LZ2,CZ61 add RZ1414 RZ114 pop 1.JUSH.1 +PWR_SRC_R- POWER_SW#_MB_USH 2.JUSH.2 NC- FPR_RST#_USH 3.JUSH.4 POA_WAKE#_R- USB20_N4_USH 4.JUSH.5 EC_FPM_EN- USB20_P4_USH 5.JUSH.17 NC- +5V_ALW 6.JUSH.21 USH_RST#_R- FPR_SCAN_INT#_R 7.JUSH.25_GND- NFC_ACTIVITY_STATUS#_R	0.1 (X00)
9	68	2018/06/08	Reserve for SSD storage protection power gate control schematic	1.add PJP1604,RN131 RZ110 for +3.3V_SSD power option 2.add RN129 for SSD protection 3.add UZ53,UZ54,RZ1471,RZ1472,CZ305,CZ306,RZ1474,QZ24(depope) 4.check SSD_SCP#,SSD_SCP_PWR_EN GPIO	0.1 (X00)
10	62	2018/06/08	add M-BIST HW Circuit	1.remove HDD_LED_MUX circuit(remove QZ2,RZ25) 2.add M_BIST circuit(DZ12,RZ1415,RZ1482,RZ1413,CZ218,QZ21,QZ3,RZ25)	0.1 (X00)
11	17	2018/06/08	BOM option for VPRO,non-VPRO	1.UC6 change to SA00005VV20(follow NB) 2.NVPRO@ RH352,RH353,UC6,CH270,RH177,RH657,RH658,RH659,RH660,UC5,RH178,RH179,RH181,RH183,RH184 3.VPRO@ UC5,RH178,RH179,RH181,RH183,RH184,UL1 4.add NVPRO_LAN_CHIP_UL1 SA00009340L 5.RZ59,RZ58,RZ60 change to 33 ohm and BOM structure NA	0.1 (X00)

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25	58	2018/07/12	GPIO modify	remove RE566,RH639,RH638,RH624,RH360,RH330,RH621,RH622,RH623,RE101,RH207,RH322,RH425 add RE340,RH661 1.UE1.D1 HDD_EN_EC → TBT RESET_N_EC 2.UE1.D6 EC_FPM_EN → FREE 3.UE1.E4 POA_WAKE# → FREE(VCI_IN3#) 4.UE1.J6 CG6 ACPI_CHECK → NB_MODE# 5.UE1.K1 PCH_PLTRST#_EC → WWAN_GPIO_CTRL 6.UE1.L8 TBT_RESET_N_EC → FPR_SCAN_INT# 7.UH1.AP21 RTD3_CIO_PWR_EN → FREE 8.UH1.AE43 NC → RTD3_CIO_PWR_EN 9.UH1.AR32 TBT_RTD3_WAKE# → NC 10.UH1.T47 NC → TBT_RTD3_WAKE# 11.UH1.BE20 LPSS_UART2_TXD → FREE 12.UH1.AW21 CNV_EN# → FREE 13.UH1.BE23 PCH_TBT_PERST# → FREE 14.UH1.AM48 FREE → PCH_TBT_PERST#	0.1 (X00)	
26	17,18	2018/07/23	3.3V_CAM_EN# change,TBT RTD3_WAKE# reserve	1. 3.3V_CAM_EN# contact to PCH GPP_D2(pin BE18) 2. Reserve 0ohm for TBT_RTD3_WAKE# to PCH GPD7(pin BE41) add RC834,RH662@,RH663 change name RH602.1 TBT_RTD3_WAKE#_GPD7 change name RH661.2 TBT_RTD3_WAKE#_K18	0.1 (X00)	
27	58	2018/07/24	remove EC VTR3 3V3 power jump	1.remove PJP21 2.+1.8V_3.3V_ALW_VTR3 → +1.8V_ALW_VTR3	0.1 (X00)	
28	44	2018/07/24	Vendor review,PD cc cap value change	CT85,CT86 470pF → 220pF RT98 0_ohm → 100k_ohm	0.1 (X00)	
29	12	2018/07/25	VCCPLL bead stuff	VCCPLL LC562 stuff,RC422 unstuff	0.1 (X00)	
30	16	2018/07/25	ESD reserve Components	reserve CH554,CE548,CC549,CH550,CH551,CH552,CC556,CH553,DA9,DA10,DZ13,CC557,CC558	0.1 (X00)	
31	17	2018/07/26	follow NB ROM part change	1.UC5_VPRO use SA00009RI10 2.UC5_NVPRO use SA00003X910 3.UC6_NVPRO use SA00005VV20	0.1 (X00)	
32	38	2018/07/31	EMI change choke size	LZ1,LI1,LI3,LI4 → SM070005U00	0.1 (X00)	
33	12	2018/07/31	power name change	1.+VCC_CORE → +IA_CORE 2.+VCC_GT → +GT_CORE 3.+VCC_SA → +SA_CORE	0.1 (X00)	
34	9	2018/08/03	change DDI port	1.(DDI1) HDMI → AR_P0 2.(DDI2) AR_P0 → AR_P1 3.(DDI3) AR_P1 → AR_P2	0.1 (X00)	
35	44	2018/08/08	Change PD controller to 65982DD	Change UT5 part to SA0000C8000 from SA0000BIJ00.	0.1 (X00)	
36	66	2018/08/08	Change ST TPM to ST33HTPH2032AHC1	Change UZ12 part to SA0000C5G10 from SA00009S040.	0.1 (X00)	
37	16	2018/08/10	follow CFL H PDG 24MHZ topology	remove RH437,direct connect	0.1 (X00)	
38	62	2018/08/14	follow NB M_BIST schematic	1.DZ12,RZ1413 unstuff 2.add RZ1482(M_BIST_R) PU +3.3V_ALW 3.CZ218 change to 2.2uF	0.1 (X00)	
39	17	2018/08/14	not support KBL H	remove RH171	0.1 (X00)	
40	56	2018/08/14	codec bom modify follow NB	RA53 stuff,RA54 unstuff	0.1 (X00)	
41	17	2018/08/14	WWAN_PWR_EN connect to PCH	1.WWAN_PWR_EN need connect to PCH pin GPP_D0 2.WWAN_PWR_EN change net name to WWAN_FULL_PWR_EN	0.1 (X00)	
42	14	2018/08/14	CNVI PDG update	RZ1382,RZ1384 change to 33 ohm,close to PCH	0.1 (X00)	
43	52	2018/08/22	naming change	1.+TS_PWR_SRC → +TS_PWR 2.remove RE361,PRIM_PWRGD → 1.8V_1.0V_PWRGD 3.RZ1483 change to unstuff	0.1 (X00)	
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44	44	2018/08/22	follow compal naming rule	TBTA_TOP_P → SW_TBT_A_USB20_P2 TBTA_TOP_N → SW_TBT_A_USB20_N2 TBTA_BOT_P → SW_TBT_A_USB20_P1 TBTA_BOT_N → SW_TBT_A_USB20_N1 TBTA_TOP_P_R → SW_TBT_A_USB20_P2_R TBTA_TOP_N_R → SW_TBT_A_USB20_N2_R TBTA_BOT_P_R → SW_TBT_A_USB20_P1_R TBTA_BOT_N_R → SW_TBT_A_USB20_N1_R		0.1 (X00)
45	52	2018/08/28	implement support 7360 card schematic	1.add component RZ1397,QZ19,RZ1398,RZ1399,UZ51,CZ216,RZ1395,RZ1396,RZ1394,RZ1403,RZ1404,CZ217,RZ1406, RZ1401,RZ1481,RZ1480,RZ1402,RZ1405,RZ1400,RZ1393,RZ1450,RE340,RC840,RC756,UZ52 2.JNGFF2.54 PCIE_WAKE# → WWAN_PEWAKE# 3.JNGFF2.67 NC → WWAN_BB_RST# 4.UE1.K1 NC → WWAN_GPIO_CTRL add GPIO UH1.BC17 → WWAN_GPIO_PERST# UH1.BF35 → WWAN_BB_RST# UH1.BD17 → WWAN_GPIO_WAKE#		0.1 (X00)
46	58	2018/08/30	align NB modify schematic	1.reserve RE821 SSD_SCP# PU to +3.3V_ALW 2.WWAN reserve RZ1484,RZ375 PU 3.reserve CN77 22U for support Teton Glacier in the future		0.1 (X00)
47	54	2018/08/30	HW internal review	1.UT11.22 UT12.22 PWD pin add test point for test 2.UZ5 remove?need HW meeting discuss 3.VCCST_PWRGD not need connect to EC,remove RE308,RE552,UE1.K10 change name to SLP_WLAN#_GATE 4.NEC_ACTIVITY_STATUS# not need connect EC to USH connect,UE1.E4 change name to VCI_IN3# 5.RE401 stuff for RTC_DET# PU to +1.8V_ALW_VTR3 6.not use LPC,remove PCH_PLTRST# EC net,remove RH244,RE375 7.remove RE560,ESPI_RESET# direct connect to JESPI 8.remove DZ7,RZ87,USH_DET# direct connect to JUSH1 9.remove NVME_LED#,SATALED#,RN100,RH380,RN101 10.for reduce power consumption,stuff RN227 11.UZ23,CZ129,CZ130 unstuff for reserve 12.JUSB2,JUSB3 VBUS add 150uF CI103,CI104 13.change name TP_DISABLE#_PTP_DISABLE#,TP_DISABLE#_R_ PTP_DISABLE#R 14.for S3 no power issue not use,remove QZ4,RZ370 15.align NB,RZ1484 stuff,RZ379 unstuff,RZ375 remove 16.remove RV1652,CV1639,name change DGPU_PWR_EN_RC_ DGPU_PWR_EN_D 17.remove QV24,RV667		0.1 (X00)
48	52	2018/09/03	WWAN_GPIO_PERST# PU power change	RZ1405 PU change to +3.3V_ALW add RZ1485 PU change to +3.3V_RUN unstuff		0.1 (X00)
49	52	2018/09/04	GPIO name change	1.HDD_EN_PCH → PCH_HDD_EN		0.1 (X00)
50	68	2018/09/04	support optane SSD add cap	1.CN60 68P_0402 change to 0.01u_0402 2.add CN80,CN81,CN84,CN82 0.01u_0402 3.add CN86 0.1u_0402		0.1 (X00)
51	18	2018/09/04	PDG eSPI series resistance update	RC366,RC367,RC368,RC369 change to 0 ohm RH97 change to 33 ohm		0.1 (X00)
52	56	2018/09/04	Space limitation,remove audio load SW	remove UZ5,PJP15,PJP16,CZ125,CZ126,CZ127,CZ128 RH345 change to @		0.1 (X00)
53	15	2018/09/05	save layout space	delete:T37,T38,RH60,RH375,RE547,RL70 downsize to 0201:RH65,RH187,CC32,RH133,RH132,RH10,RH11,RH13,RH14,RH15,RH16,RH17,RH309, RH316,RH378,RH348,RH350,RH441,RH203,RH204,RH424,RH309 change to test point:RH99(T424)		0.1 (X00)
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68	62	2019/01/03	DFX request	15" add Fiducial Mark FD8	0.3 (X02)
69	52	2019/01/03	RF BOM option	1.LI9 depop 2.RI49,RI50 change to use SM01000TP00 3.RI49,RI50 change name to LI49,LI50	0.3 (X02)
70	58	2019/01/03	reserve the CNVi detect on GPP_D20	1.remove test point T269 2.reserve 0 ohm RE828 3.RE828.1 CNVI_EN# connect to PCH GPP_D20 4.RE828.2 connect to CNV_DET#_EC 5.CNVI_EN# reserve 75K PD(RH868)	0.3 (X02)
71	52	2019/01/03	INTEL suggest REFCLK_CNV need impedance control	1.remove 0 ohm RZ371,RZ81 2.remove net ISH_UART0_RXD,ISH_UART0_TXD,ISH_UART0_CTS#,ISH_UART0_RTS#	0.3 (X02)
72	56	2019/01/03	DFX request	DA4,DA5 change footprint to 1N4148WS-7-F_SOD323-2	0.3 (X02)
73	59	2019/01/03	board ID change to X02	board ID RE79 change to X02 62K ohm	0.3 (X02)
74	38	2019/01/03	align NB reserve fuse	1.reserve FZ4,FZ5,RZ1486 2.add RZ1487,RZ1488 0 ohm	0.3 (X02)
75	23,24	2019/01/03	DFX request	JDIMM1,JDIMM2 change footprint to FOX_ASAA821-H4RB5-7H_260P	0.3 (X02)
76	38	2019/01/03	to avoid camera & DMIC lost after ESD test	pop DA9,DA10	0.3 (X02)
77		2019/01/03	0 ohm change to short pad	location reference X10 BH DVT2.0 0 Ohm_190104.xlsx	0.3 (X02)
78	66	2019/01/03	align LKE reserve TPM power source	+3.3V_VPS_UZ12 reserve 0 ohm RZ1489 to +3.3V_ALW	0.3 (X02)
79	38,58	2019/01/03	ESD request	reserve cap 0.1u TOUCH_SCREEN_PD#_R (CV113) CAM_MIC_CBL_DET# (CV112) BIA_PWM (CV111) EDP_HP (CV110) TOUCH_SCREEN_DET# (CV109) IR_CAM_DET# (CZ1203) CE548 from 0.1u 0201 change to 4700p 0402	0.3 (X02)
80	7,38	2019/01/03	ESD request	CC306,CC308,CC302,CH551,CC305,CC304,CC303,CV113,CV112,CV110,CV109,CZ1203 from reserve to add 0.1uF cap CE548 from 47nF reserve to add 47nF	0.3 (X02)
81	7,18	2019/01/03	ESD request	RC124 depop,CC307 100pf pop CH266 100 pf POP	0.3 (X02)
82	52	2019/01/03	BOM option for non WWAN SKU	HU non WWAN SKU BOM option 1.LI8,LI16,LI17,CZ198,CZ42,CZ41,CZ23~CZ26 change to WWANREF 2.UZ29,CZ154,CZ155,RZ360,CZ150,CZ151,CZ152,CZ153,CZ110,CZ111,RZ43,DZ5,DZ6,CZ37,RZ1406,CZ217,UZ52,RZ1405,RZ1400,UZ51,CZ216,QZ19,RZ1399,RZ1397,QZ8,CZ17~CZ21 change to WWAN@	0.3 (X02)

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83	ALL	2019/03/06	0 ohm change to short pad	follow pilot 0 Ohm_190305 table to modify	1.0 (A00)
84	18	2019/03/06	remove service mode switch for MP	depop SW1, RH101 short pad RH100	1.0 (A00)
85	59	2019/03/06	board ID change	RE79 change to 4.3k	1.0 (A00)
86	ALL	2019/03/06	DFX request,add green paint	footprint add "-NPM" 15HD:CMOS1,FZ5,FZ4,RZ1486,LV3,LV6,LV9,LV12,RH238,RC422,RI47,RI48,LI9,RI27,RI28,RI29,RI30,CI104,RZ96,RH289,LI11,LI12,LI13,CI103 15HU:CMOS1,FZ5,FZ4,RZ1486,LV3,LV6,LV9,LV12,RH238,RC422,RI47,RI48,LI9,RI27,RI28,RI29,RI30,CI104,RZ96,RZ108,RZ102 14HD:CMOS1,FZ5,FZ4,RZ1486,LV3,LV6,LV9,LV12,RC422,RI47,RI48,LI9,RI27,RI28,RI29,RI30,CI104,CI103,CI32 14HU:CMOS1,FZ5,FZ4,RZ1486,LV3,LV6,LV9,LV12,RH238,RC422,RI47,RI48,LI9,RI27,RI28,RI29,RI30,CI104,RH289,CI103,CI32,CI104	1.0 (A00)
87	52	2019/03/06	Align NB schematic	Change RZ43 from 47K_0402_5% to 10K_0402_5%	1.0 (A00)
88	51	2019/03/06	DFB suggest modify UL1 pad layout dimension to 6.6*6.6mm	UL1 change footprint to WGI219LM-SLKJ3-A0_QFN48_6X6	1.0 (A00)
89	52	2019/03/06	align NB change UZ52 power rail from 3.3V_RDN to 3.3V_ALW	RZ1403 depop,RZ1404 pop and keep 0 ohm	1.0 (A00)

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